

Winery CALPELLA N11M-GE Schematics

Mobile Arrandale

Intel Ixex Peak-M

2009-09-09

REV : SA

DY : Nopop Component

UMA : Pop when schematic is UMA

DIS : Pop when schematic is DIS

<Core Design>



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Custom	Vostro Calpella	SA			
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Winery CALPELLA Block Diagram

Project code : 91.4ET01.001
Part Number : 48.4ET05.0SA
PCB P/N : 09289
Revision : SA

PCB LAYER

- L1: Top
- L2: VCC
- L3: Signal
- L4: Signal
- L5: GND
- L6: Bottom

Clock Generator
SLG8SP585

VRAM(gDDR3)
64Mb x 16 x 4 (512MB)

Nvidia
NI1M-GE(40nm)

100MHz/
2.5Gbps
PCIe x 16
Bandwidth
: 8GB

Intel CPU
Arrandale

8,9,10,11,12,13,14

DDRIII 1066 Channel A
800/1066MHz
DDR III 1066 Channel B
800/1066MHz

DDRIII Slot 0
1066
DDRIII Slot 1
1066

Power SW
TPS2231R

New Card
(On daughter board)

10/100/1000LOM
RTL8111DL
(On daughter board)

RJ45
CONN

Mini-Card
802.11a/b/g/n
Mini-Card
WWAN/ WIMAX

Touch Panel
(only for 15")
Left Side:
USB x 2
Right Side:
USB x 1
CAMERA
Bluetooth
Biometric

Free fall sensor
TPM
(On daughter board)

KBC
NUVOTON
NPCE781BA0DX

Flash ROM
256kB
Touch PAD
Int. KB

Thermal & Fan
EMC2102

Capacity Board
(On daughter board)

Intel PCH

14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIe ports (8)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE

20, 21, 22, 23, 24, 25, 26, 27, 28

DMIX4
2.5 GT/s
FDI (UMA)
2.7 GT/s

PCIe
100MHz
2.5Gbps
USB 2.0
480Mbps

SM Bus
400KHz
LPC Bus
33MHz

SATA, USB
SATA
3Gbps
SATA
3Gbps
SATA
3Gbps

USB,ESATA
Multi-Port x1
ODD
HDD
Flash ROM
4MB

CardReader

Realtek
RTSS138

USB 2.0
480Mbps

(8 in 1)SD/MMC
MS/MS Pro/xD

Digital Mic Array

Azalia
CODEC
OP AMP
IDT
92HD81

MIC IN
HP OUT

2CH SPEAKER

SYSTEM DC/DC
ISL62883

INPUTS
+PWR_SRC
OUTPUTS
+VCC_CORE

SYSTEM DC/DC
TPS51125

INPUTS
+PWR_SRC
OUTPUTS
+15V_ALW
+3.3V_RTC_LDO
+5V_ALW
+3.3V_ALW

SYSTEM DC/DC
TPS51116

INPUTS
+PWR_SRC
OUTPUTS
+1.5V_SUS
+0.75V_DDR_VTT
+V_DDR_MCH_REF

SYSTEM DC/DC
ADP3211

INPUTS
+PWR_SRC
OUTPUTS
+CPU_GFXCORE

SYSTEM DC/DC
TPS51218

INPUTS
+PWR_SRC
OUTPUTS
+VCC_GFX_CORE

CHARGER
BQ24745

INPUTS
+DC_IN
+PBATT
OUTPUTS
+PWR_SRC

SYSTEM DC/DC
TPS51218

INPUTS
+PWR_SRC
OUTPUTS
VTT_CORE

LDO
APL5930

INPUTS
+3.3V_ALW
OUTPUTS
+1.8V_RUN

LDO
RT9025

INPUTS
+3.3V_ALW
OUTPUTS
+1.8V_RUN_GPU

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Block Diagram

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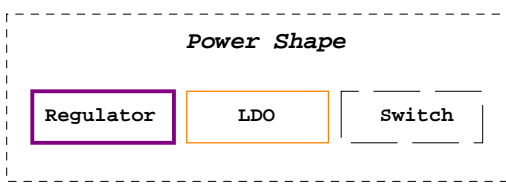
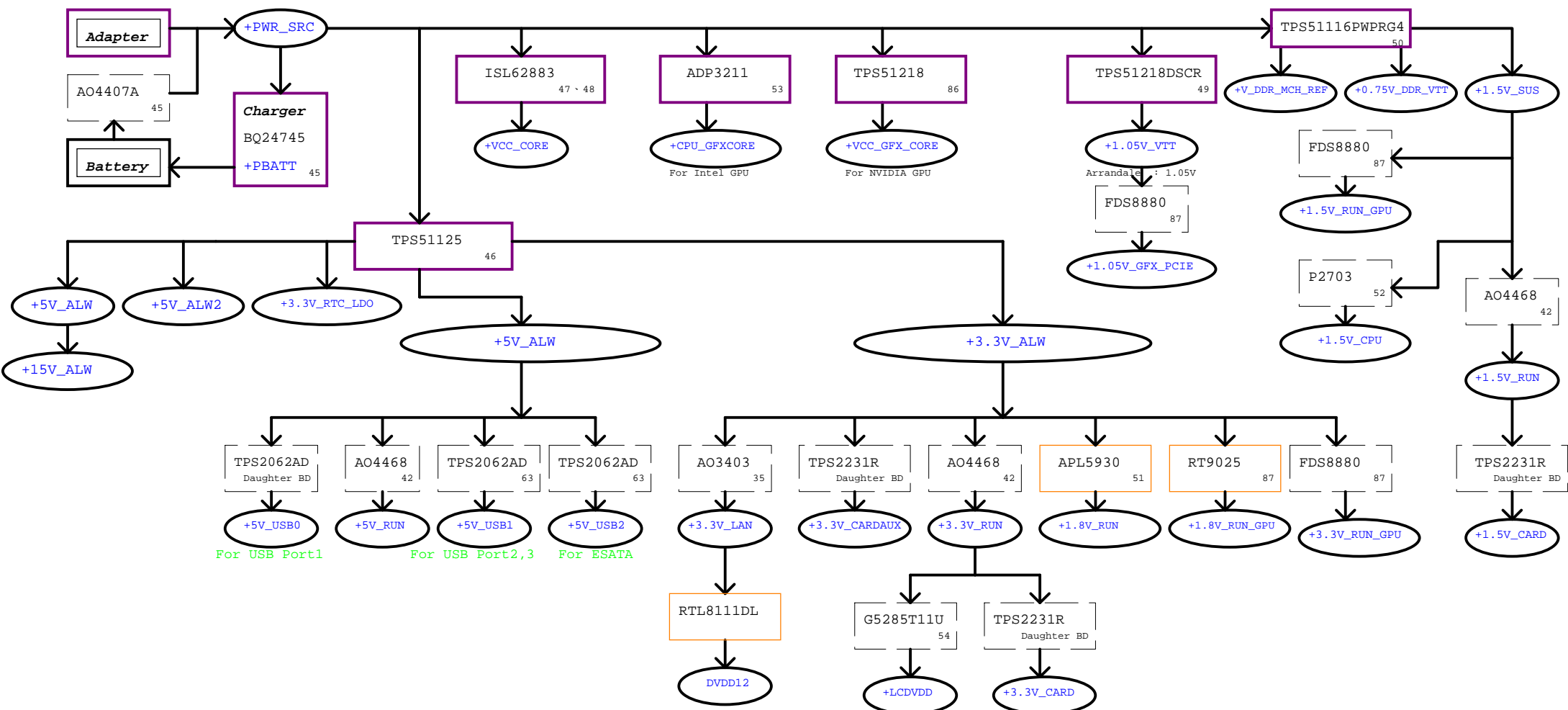
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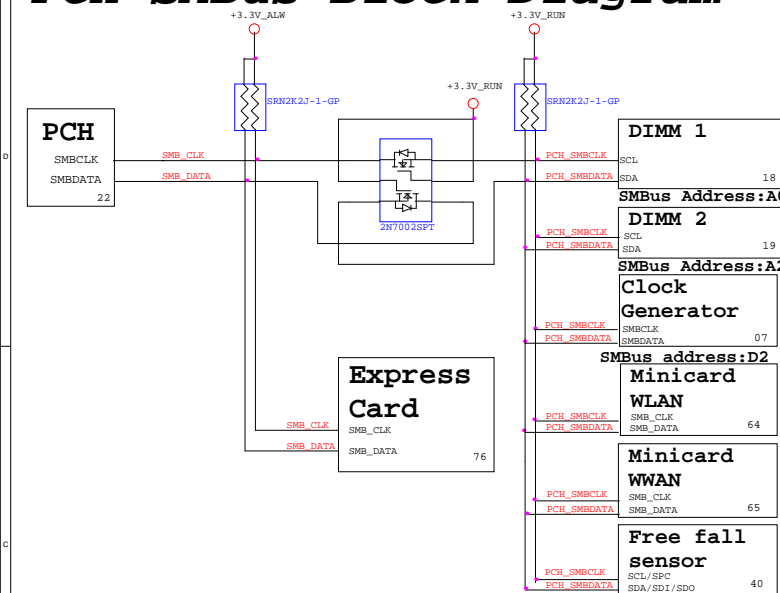
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<div style="text-align: center;"> LDO RT9025 </div> <div style="text-align: right;">87</div>	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN_GPU

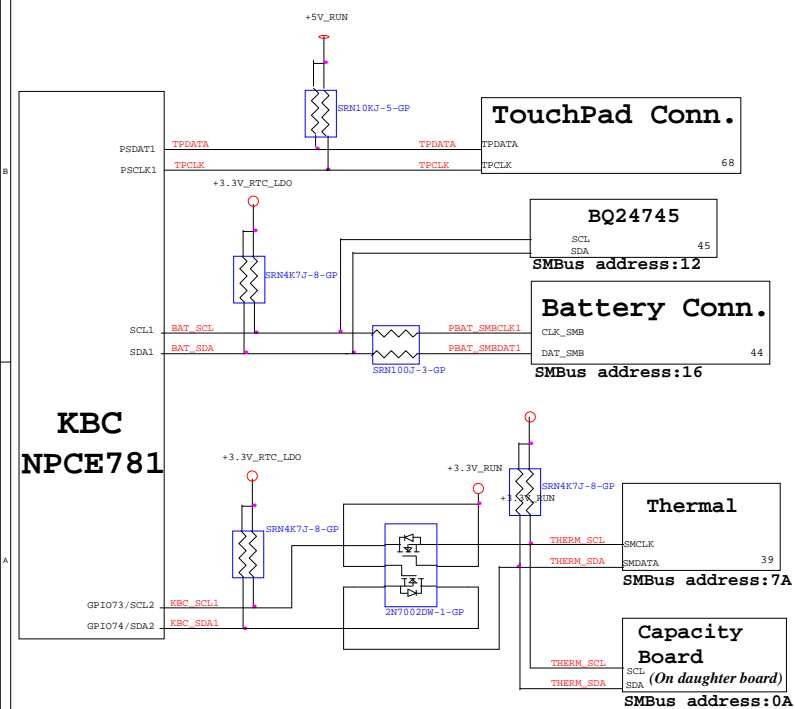
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Block Diagram			
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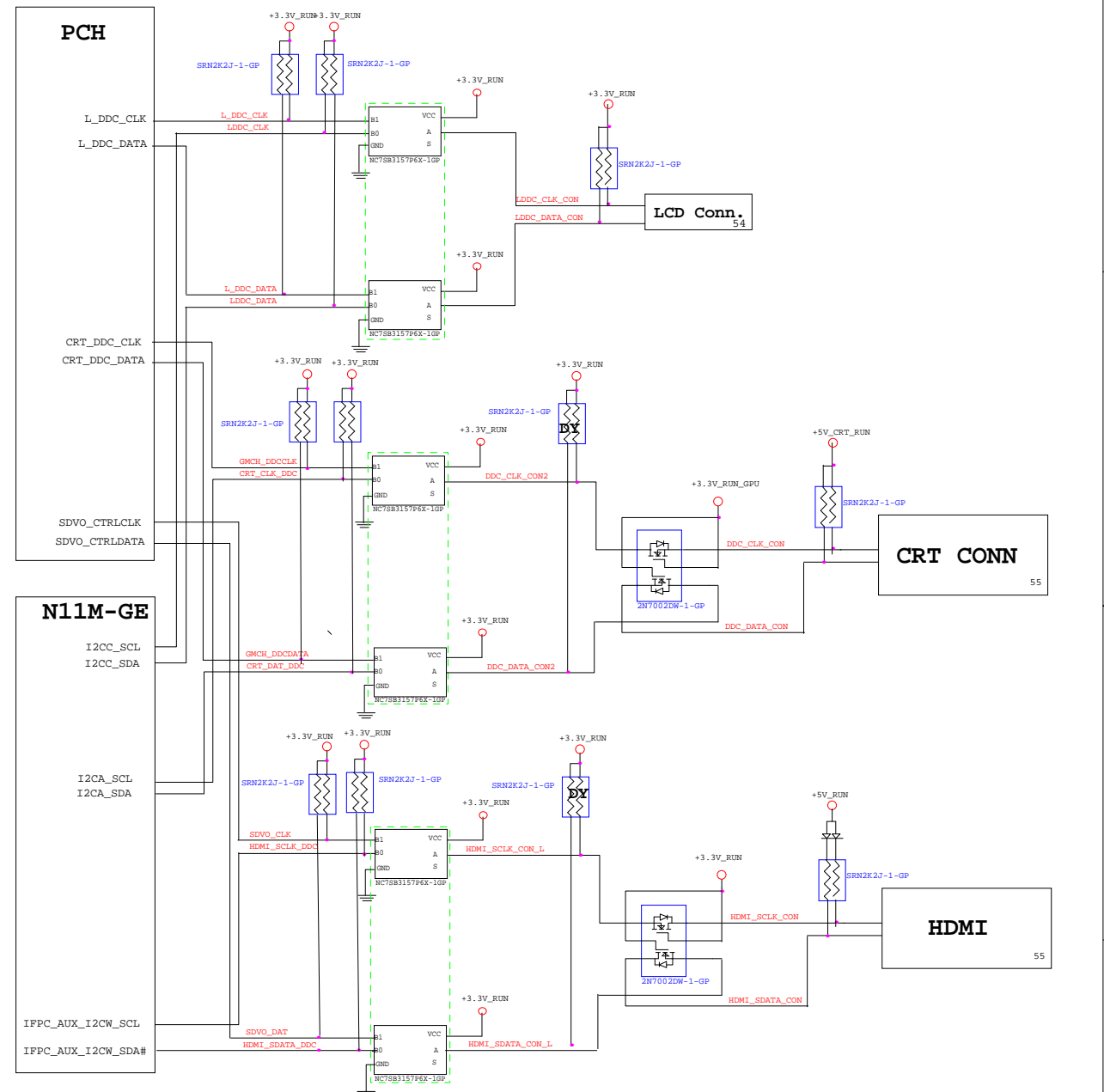
PCH SMBus Block Diagram



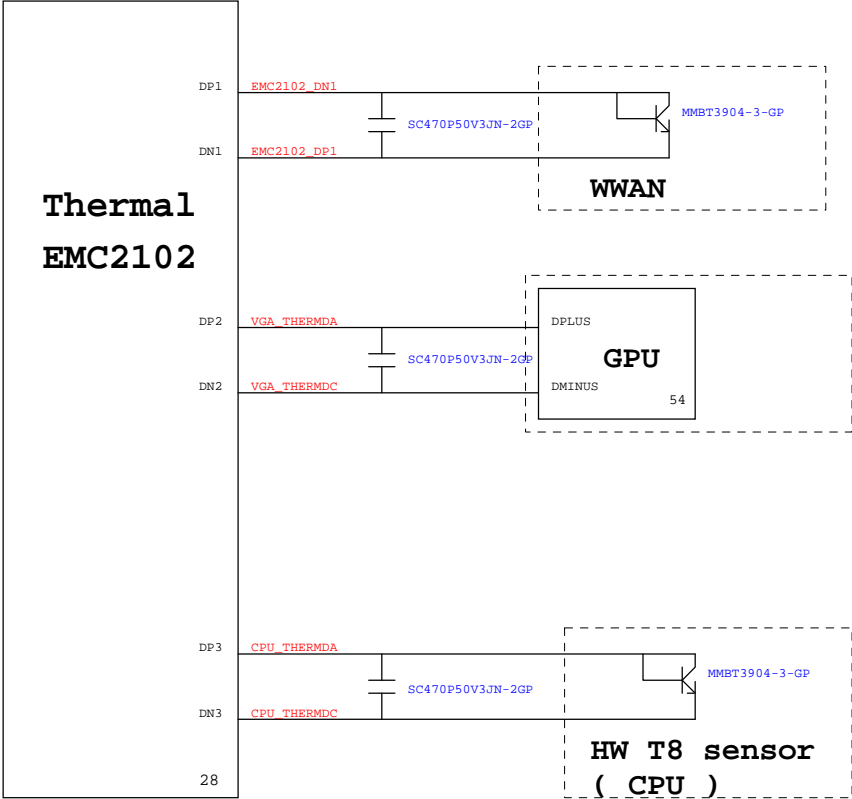
KBC SMBus Block Diagram



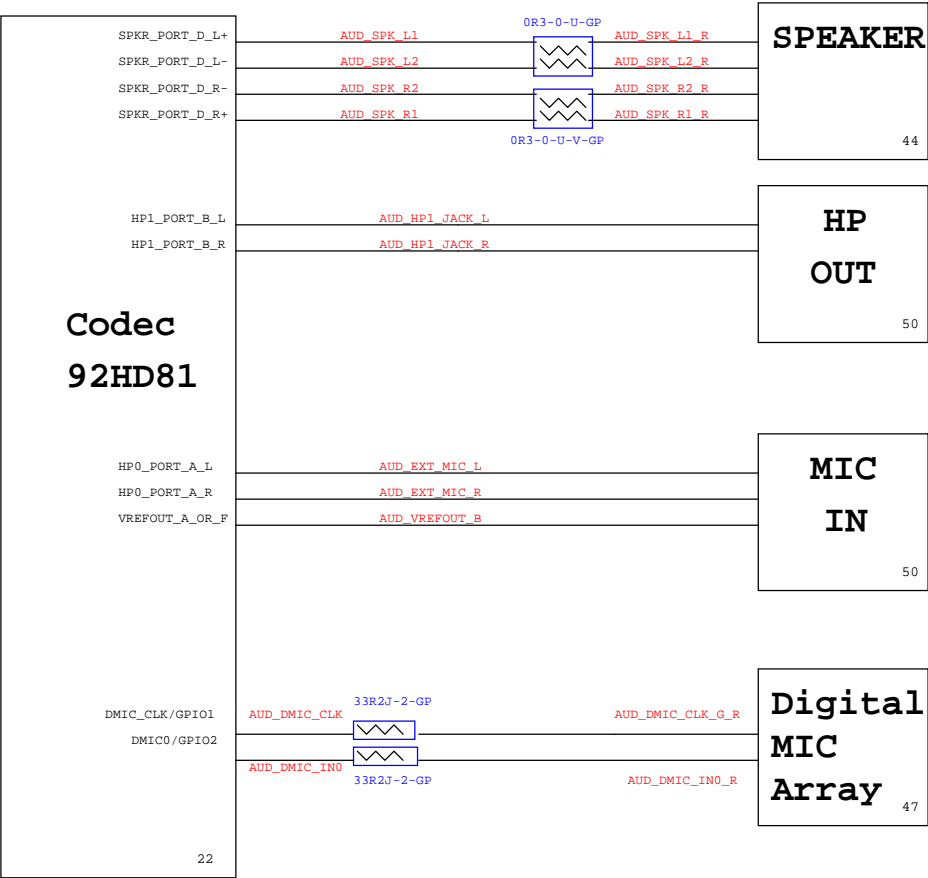
Switchable Graphic SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap ModeNote: Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 k do not stuff resistor.
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#/GPIO51	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing

LANE1	Card reader
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	MiniCard WWAN
LANE5	New Card

Processor Strapping

Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

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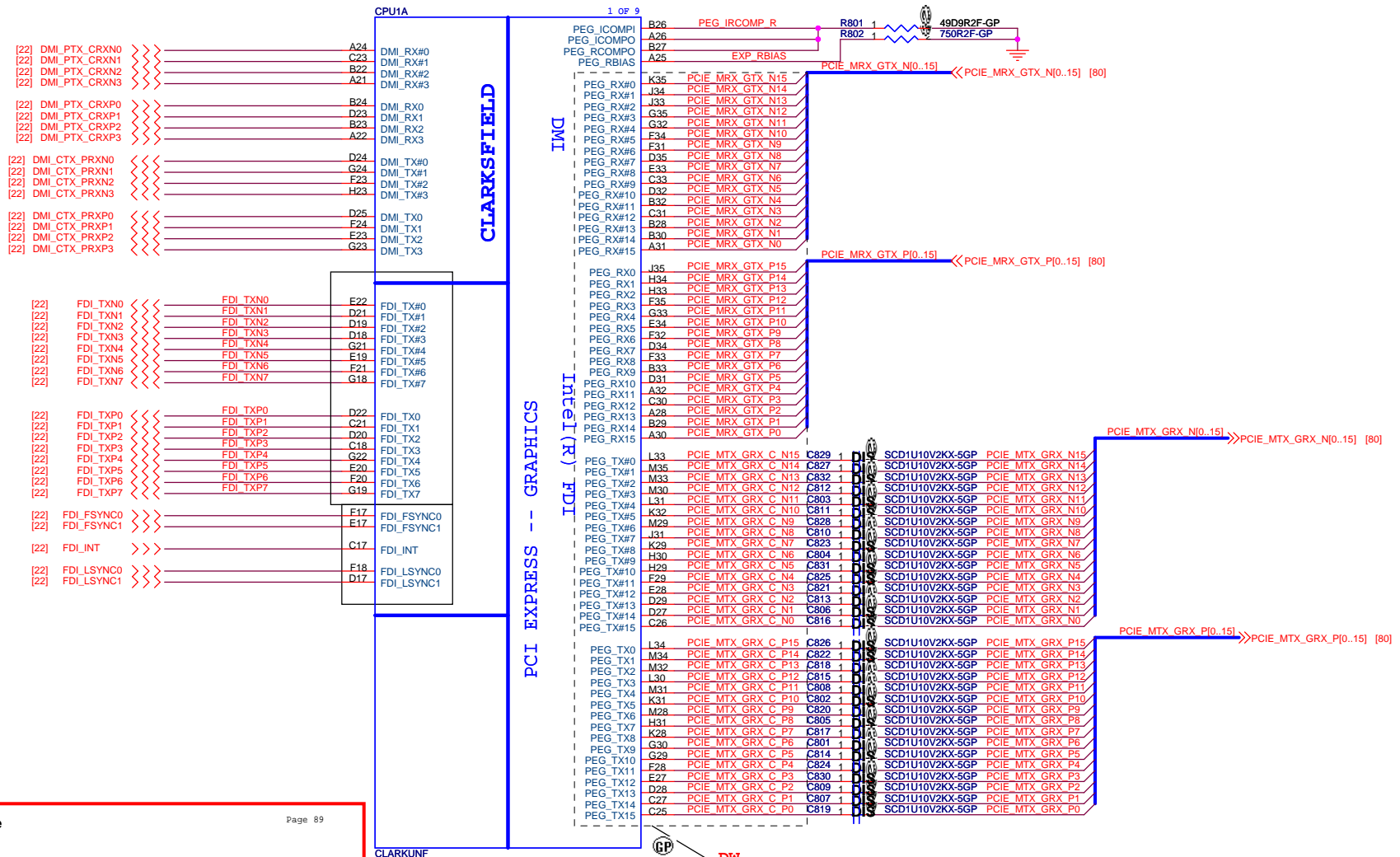
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Calpella Platform Design Guide Revision 1.6

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2.4 Arrandale Graphics Disable Guideline

It applies to Arrandale and Clarksfield discrete graphic designs.

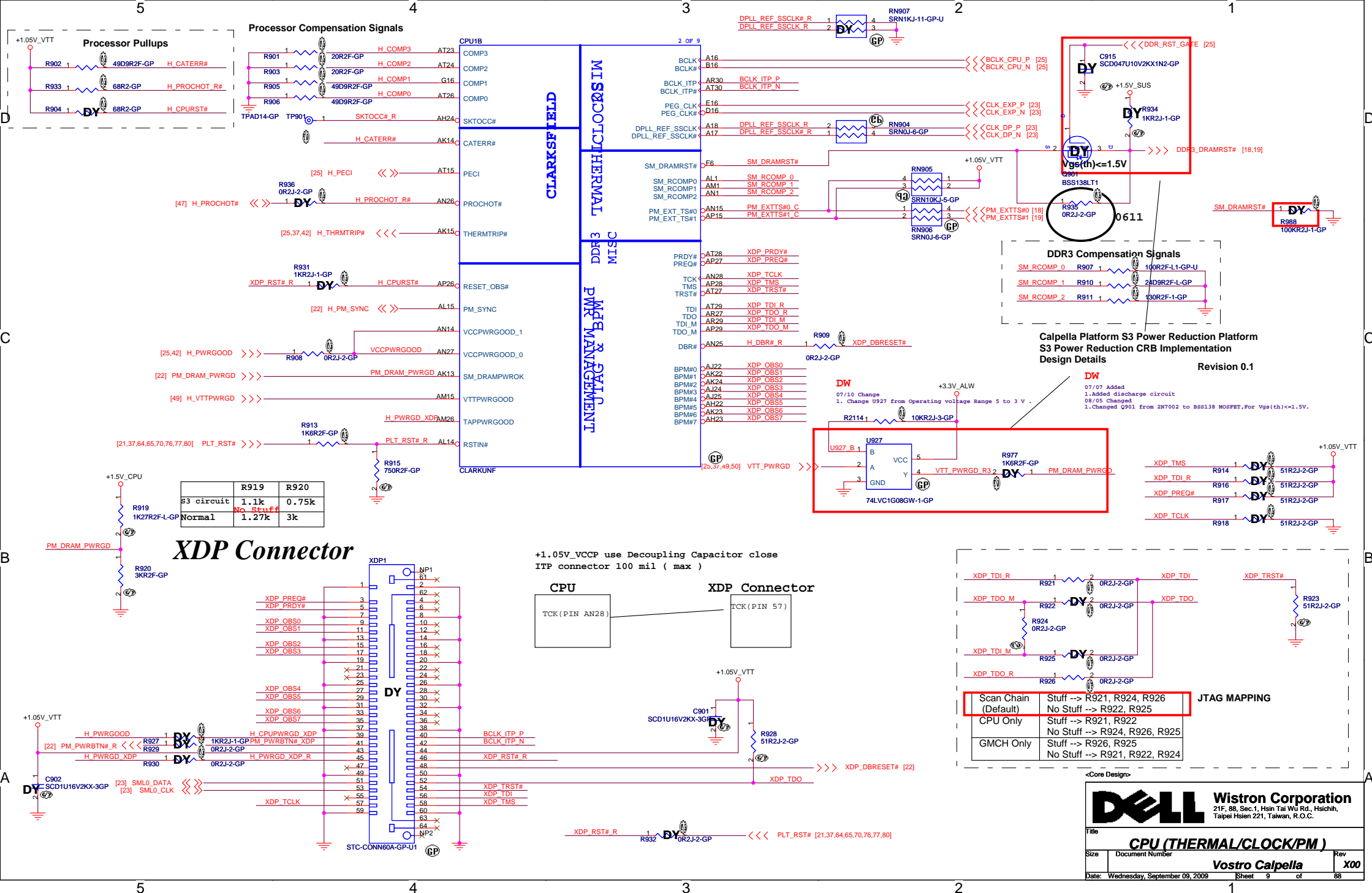
FDI_TX[7:0] and FDI_TX# [7:0] can be left floating on the Arrandale. The GFX_IMON, FDI_FSYN0, FDI_FSYN1, FDI_LSYN0, FDI_LSYN1, and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

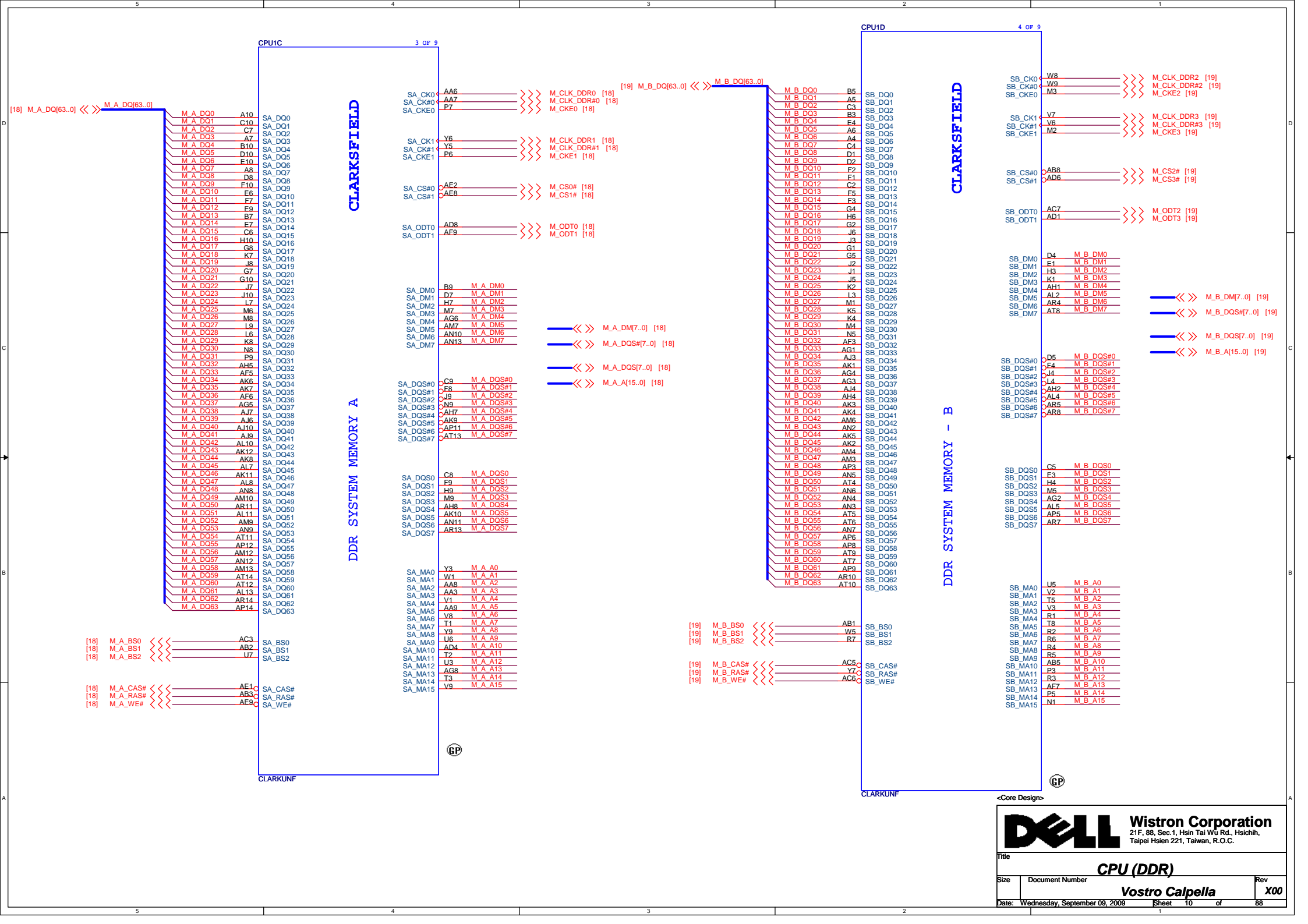
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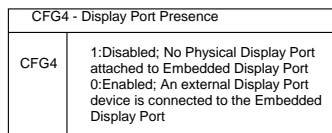
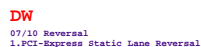
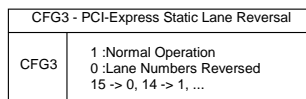
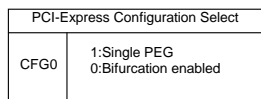
07/02 Added
1. Added Flexible Display Interface (Intel® FDI) commentariat

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CPU (PCIe/DMI/FDI)			
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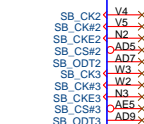
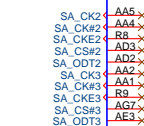
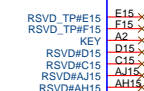
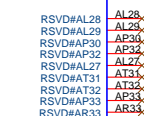
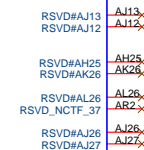
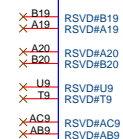
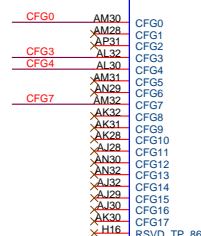
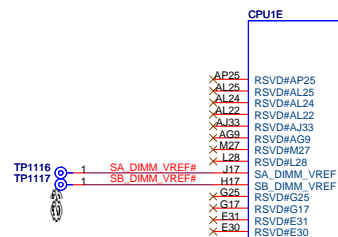
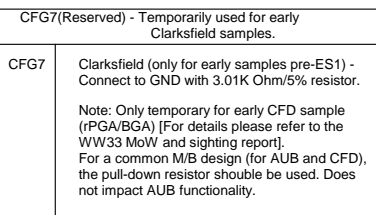
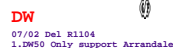




Switchable GFX, just like integrated GFX only, to enable LVDS it is required that the OEM set the LDVS (L_DDC_DATA) strap to present (pulled up) and the eDP strap (CFG[4]) to disabled (not pulled down).

eDP for Switchable GFX can only be driven out of Port D of PCH. To configure Port D for embedded DP it is required to set the `DDPD_CTRLDATA` strap high to 3.3V Core rail through 2.2 k Ω \pm 5% resistor, `LVDS (L_DDC_DATA)` strap as no connect and the eDP strap `CFG[4]` as no connect.

Page 482.486



VSS (AP34) can be left NC in CRB implementation; EDS/DG recommendation to GND.

DELL

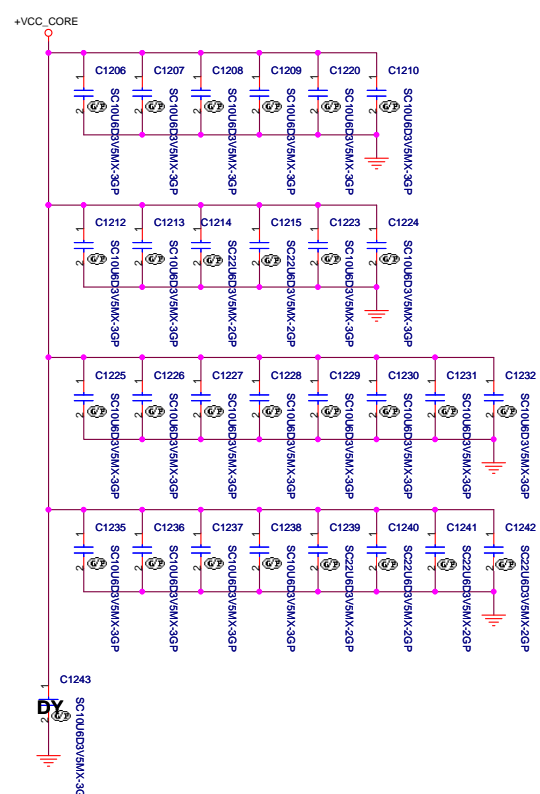
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+VCC_CORE

48A

PROCESSOR CORE POWER



48A

- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG31 VCC
- AG30 VCC
- AG29 VCC
- AG28 VCC
- AG27 VCC
- AG26 VCC
- AF35 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AF26 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
- AC33 VCC
- AC32 VCC
- AC31 VCC
- AC30 VCC
- AC29 VCC
- AC28 VCC
- AC27 VCC
- AC26 VCC
- AA35 VCC
- AA34 VCC
- AA33 VCC
- AA32 VCC
- AA31 VCC
- AA30 VCC
- AA29 VCC
- AA28 VCC
- AA27 VCC
- AA26 VCC
- Y35 VCC
- Y34 VCC
- Y33 VCC
- Y32 VCC
- Y31 VCC
- Y30 VCC
- Y29 VCC
- Y28 VCC
- Y27 VCC
- Y26 VCC
- U35 VCC
- U34 VCC
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- R32 VCC
- R31 VCC
- R30 VCC
- R29 VCC
- R28 VCC
- R27 VCC
- R26 VCC
- P35 VCC
- P34 VCC
- P33 VCC
- P32 VCC
- P31 VCC
- P30 VCC
- P29 VCC
- P28 VCC
- P27 VCC
- P26 VCC

CLARKSFIELD

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINE

CLARKUNIF

- VTT0 AH14
- VTT0 AH11
- VTT0 AH10
- VTT0 J14
- VTT0 L13
- VTT0 H14
- VTT0 H12
- VTT0 G14
- VTT0 G13
- VTT0 G12
- VTT0 G11
- VTT0 E14
- VTT0 E13
- VTT0 E12
- VTT0 D14
- VTT0 D13
- VTT0 D12
- VTT0 D11
- VTT0 C14
- VTT0 C13
- VTT0 C12
- VTT0 B14
- VTT0 B12
- VTT0 A14
- VTT0 A13
- VTT0 A12
- VTT0 A11

- VTT0 AF10
- VTT0 AE10
- VTT0 AC10
- VTT0 AB10
- VTT0 Y10
- VTT0 W10
- VTT0 U10
- VTT0 T10
- VTT0 J12
- VTT0 J11
- VTT0 J16
- VTT0 J15

PSI# AN33 >>> PSI# [47]

AK35 CPU_VID0 >>> CPU_VID[6..0] [47]

AK33 CPU_VID1

AK34 CPU_VID2

AL35 CPU_VID3

AL33 CPU_VID4

AM33 CPU_VID5

AM35 CPU_VID6

AM34 >>> PM_DPRSLPVR [47]

PROC_DPRSLPVR

VTT_SELECT G15 TP_H_VTTVID1 TP1203 TPAD14-GP

H_VTTVID1 = Low, 1.1V

H_VTTVID1 = High, 1.05V

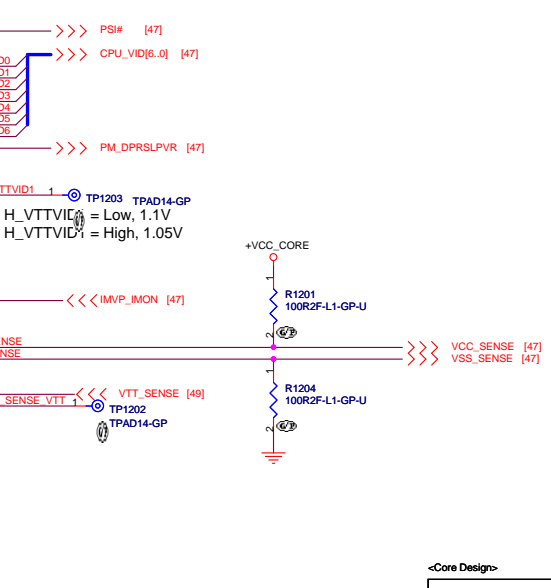
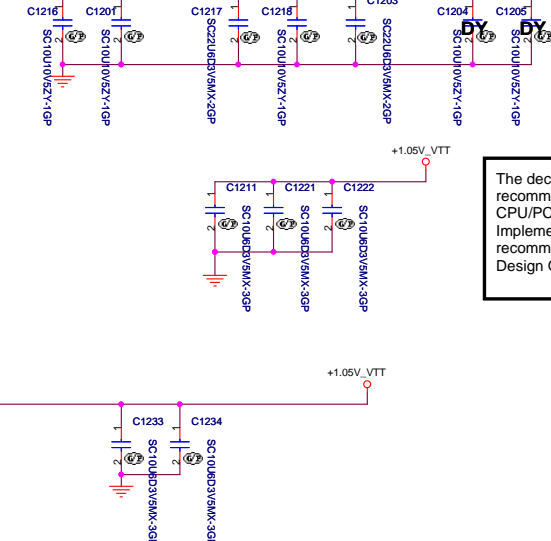
ISENSE AN35 <<< IMVP_IMON [47]

VCC_SENSE AJ34 VCC_SENSE [47]

VSS_SENSE AJ35 VSS_SENSE [47]

VTT_SENSE B15 TP_VSS_SENSE_VTT TP1202 TPAD14-GP

VSS_SENSE_VTT A15



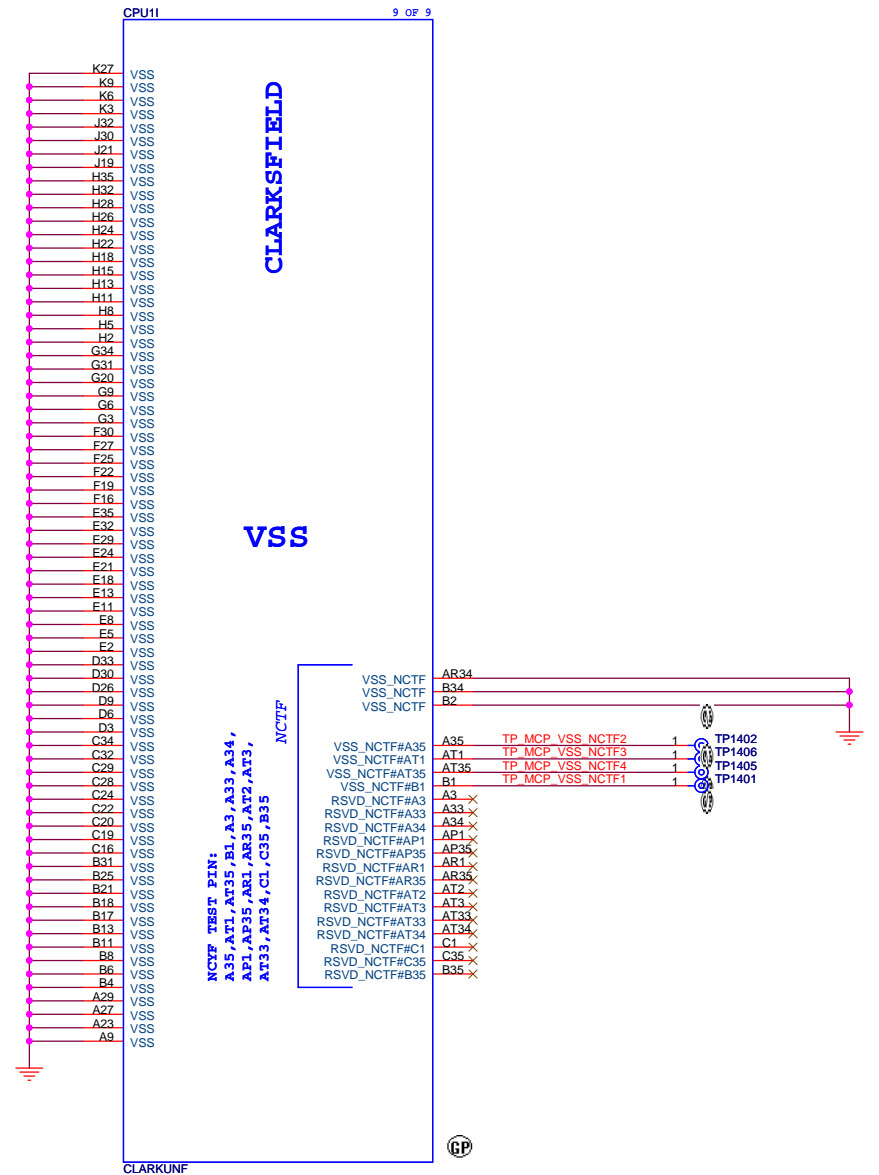
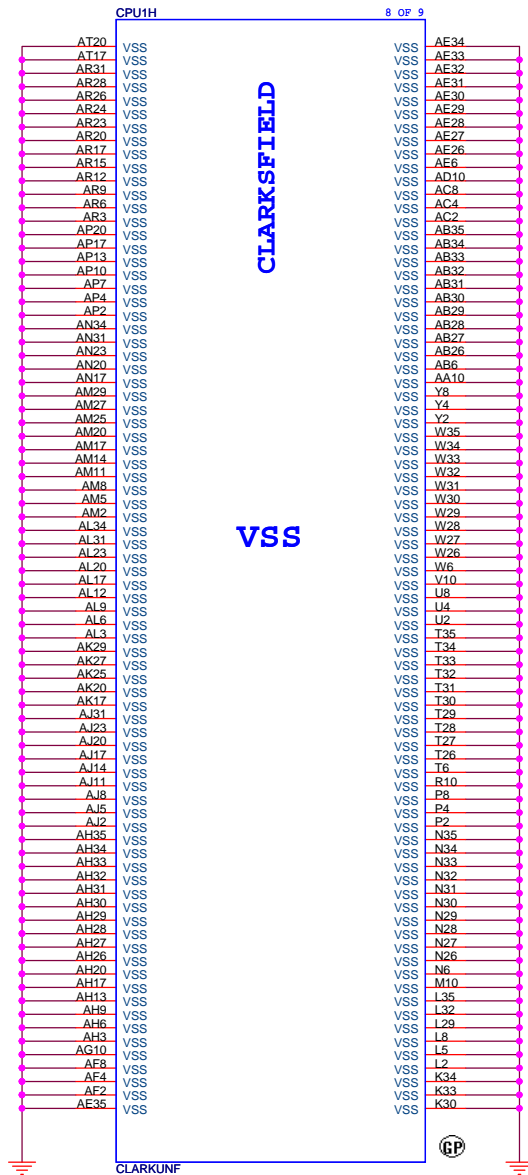
The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Arrandale VTT=1.05V; Clarksfield VTT=1.1V

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CPU (VSS)


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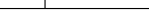
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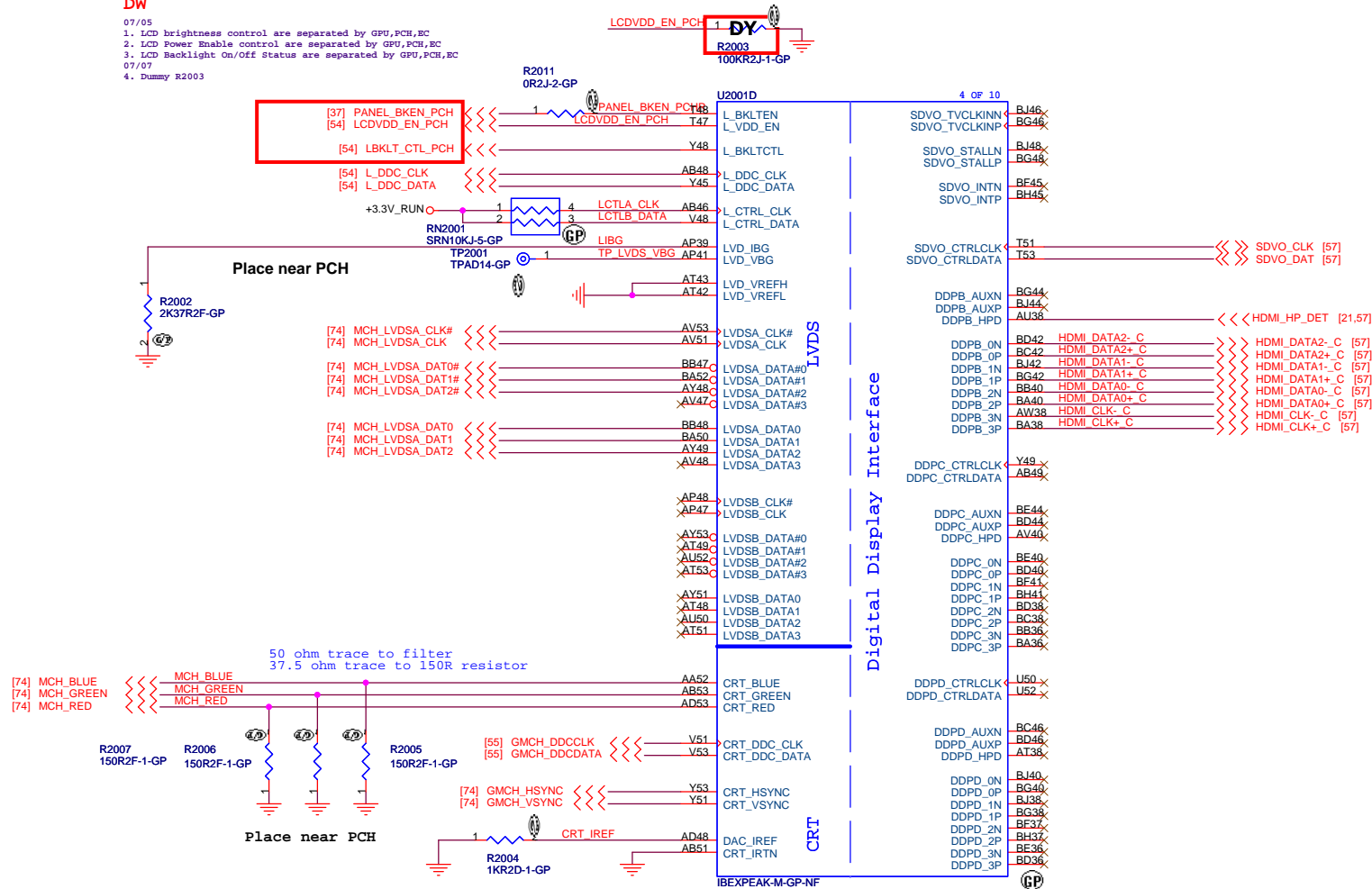
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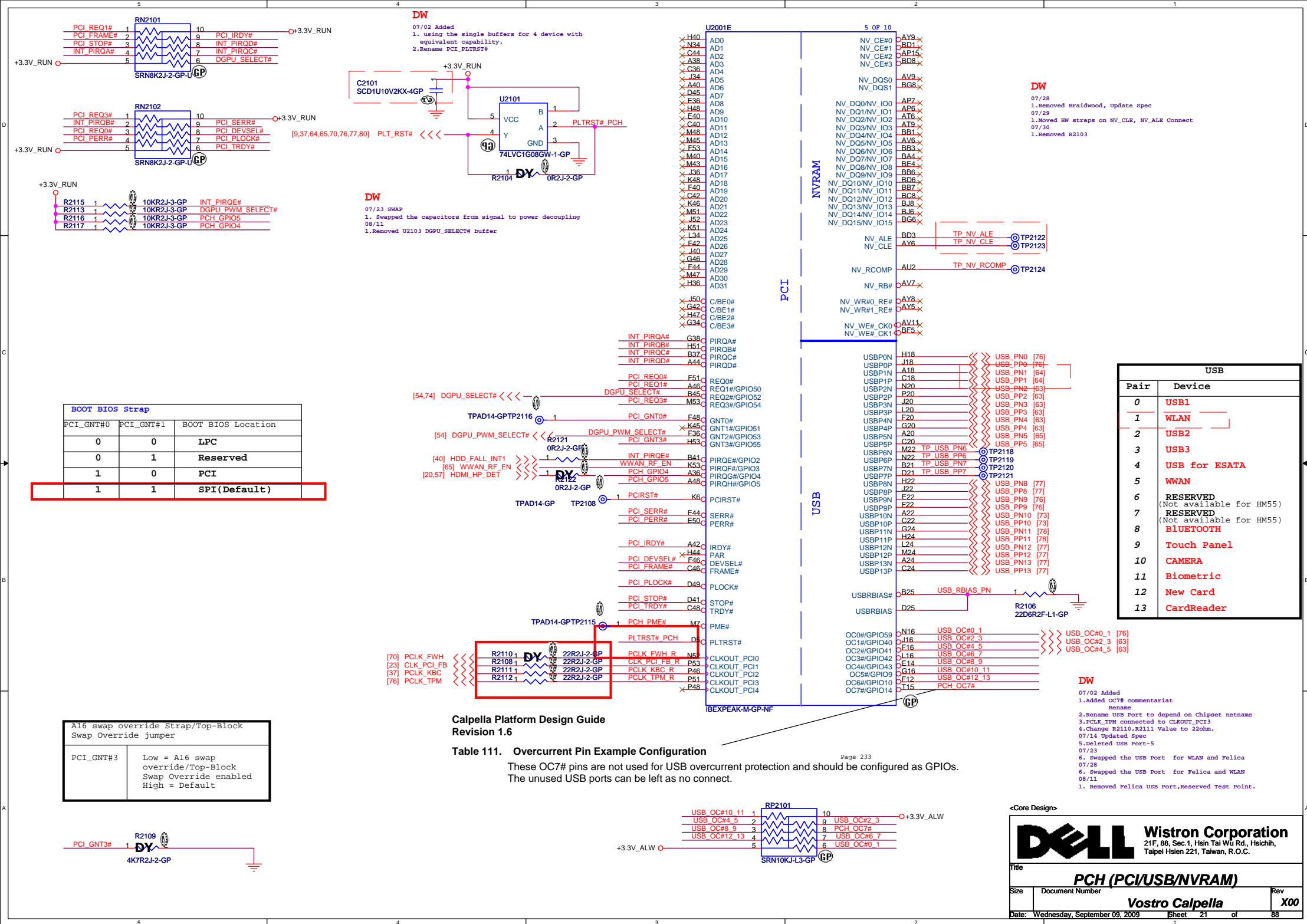
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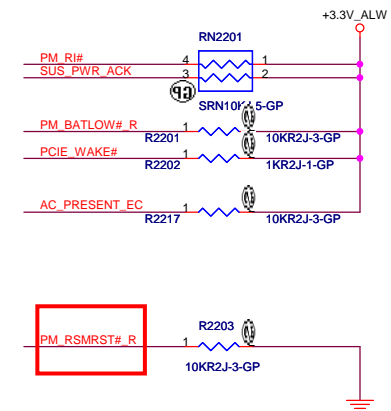
07/05

1. LCD brightness control are separated by GPU,PCH,EC
2. LCD Power Enable control are separated by GPU,PCH,EC
3. LCD Backlight On/Off Status are separated by GPU,PCH,EC
- 07/07
4. Dummy R2003

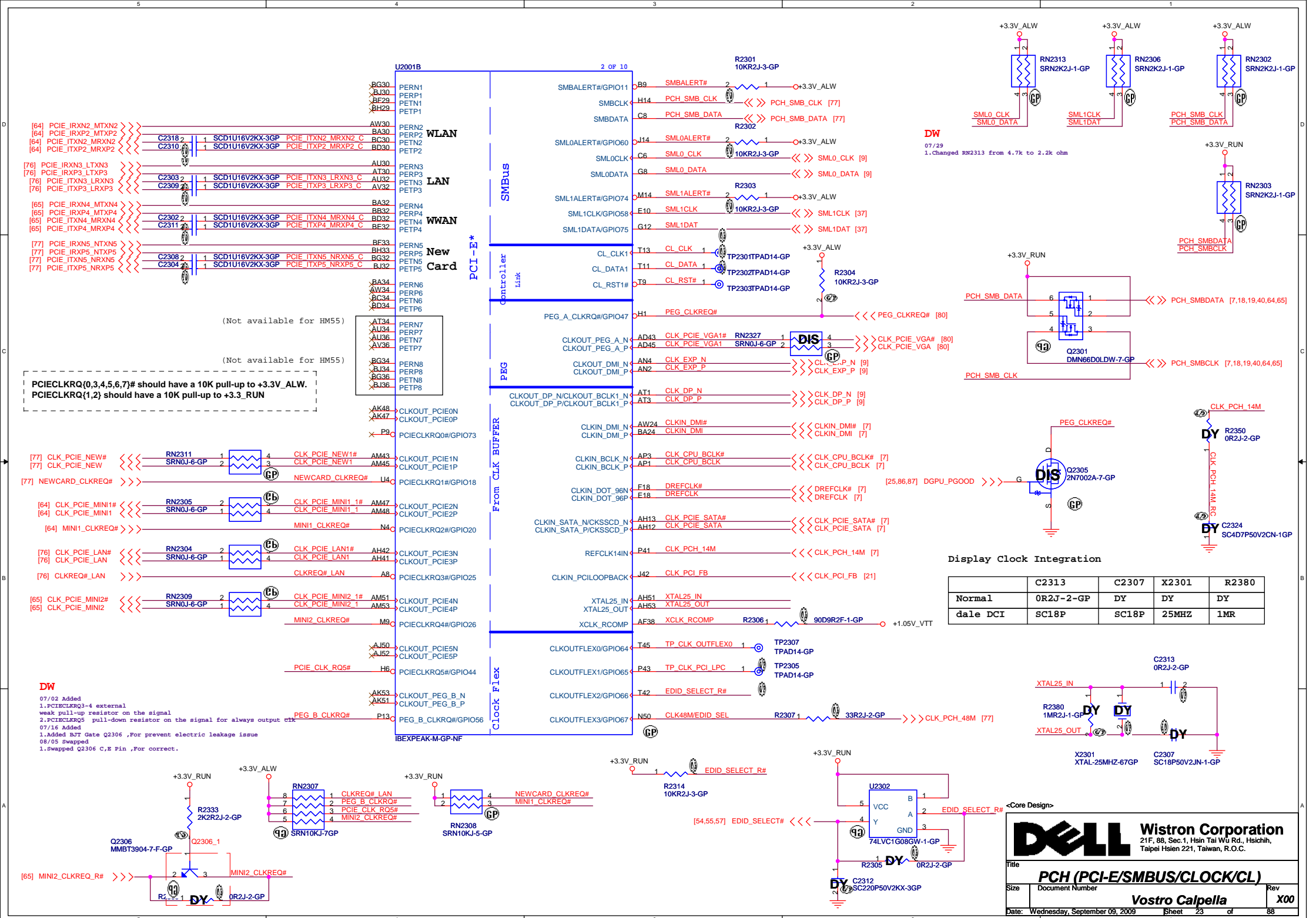


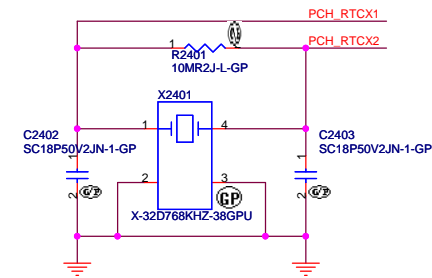
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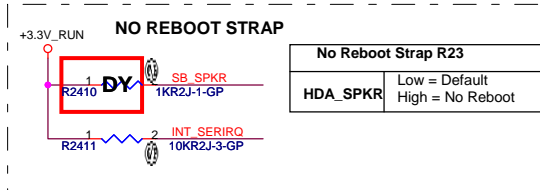
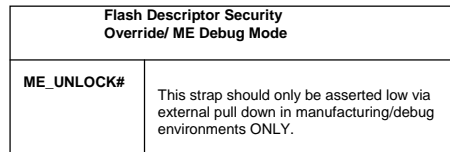
07/02 Modified
1.Modified PM RSMRST# R signal to on pull-down resistor connect





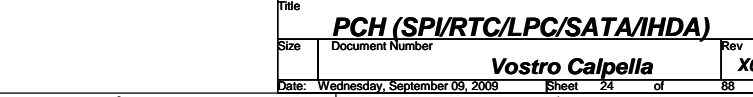
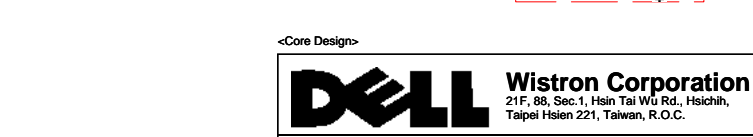
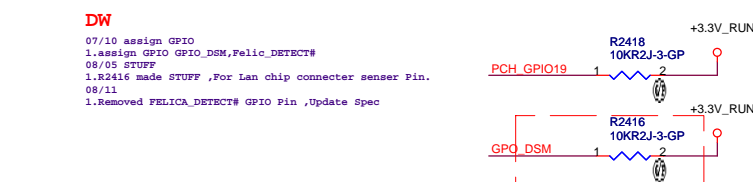
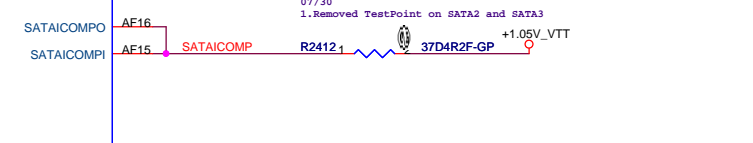
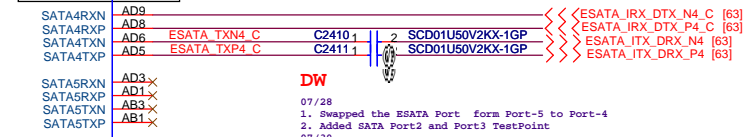
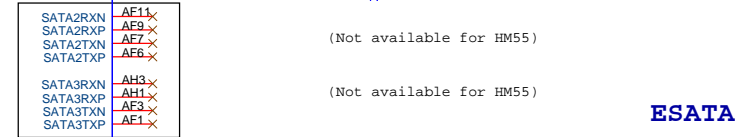
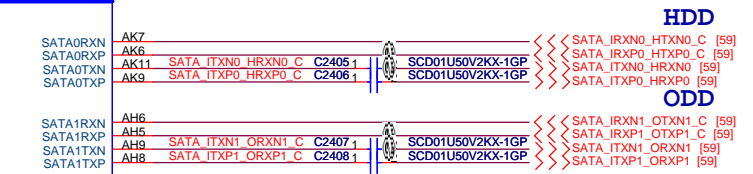
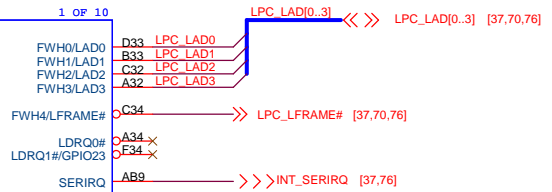
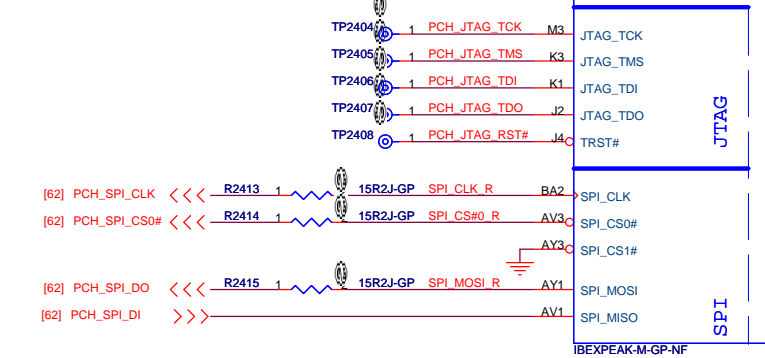
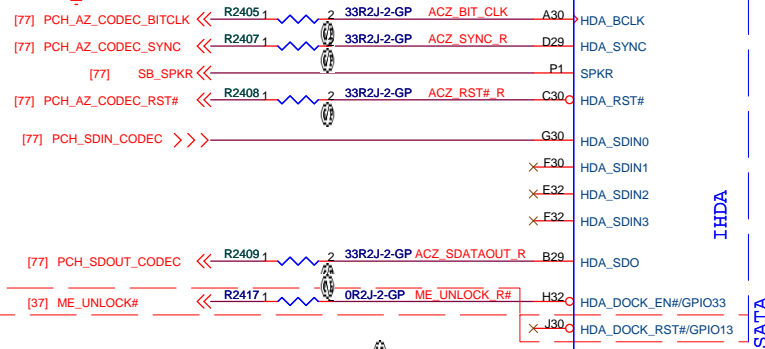
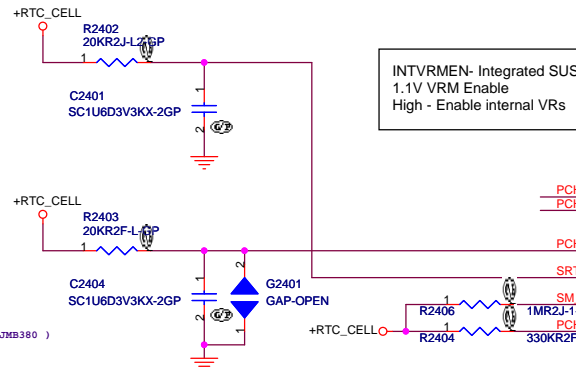
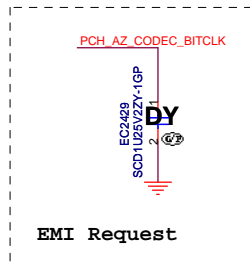
DW

07/23 Added
1. Added "ME in Manufacturing Mode" strap
2. Added CardReader_Make# to sent Card detect signal for PCH . (Only For JMB380)
07/30
1. Changed R2403 tolerance from 5% to 1%.



DW

07/02 Change
1. Change R2410 to dummy
08/18
1. Removed PCH_GPIO13 not in use



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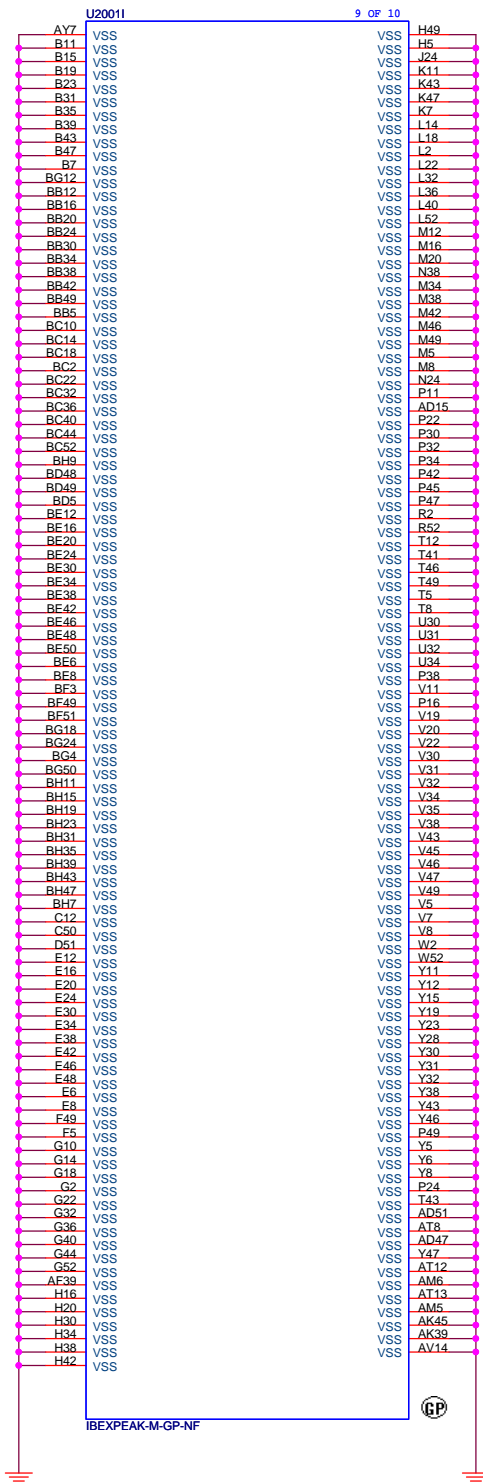
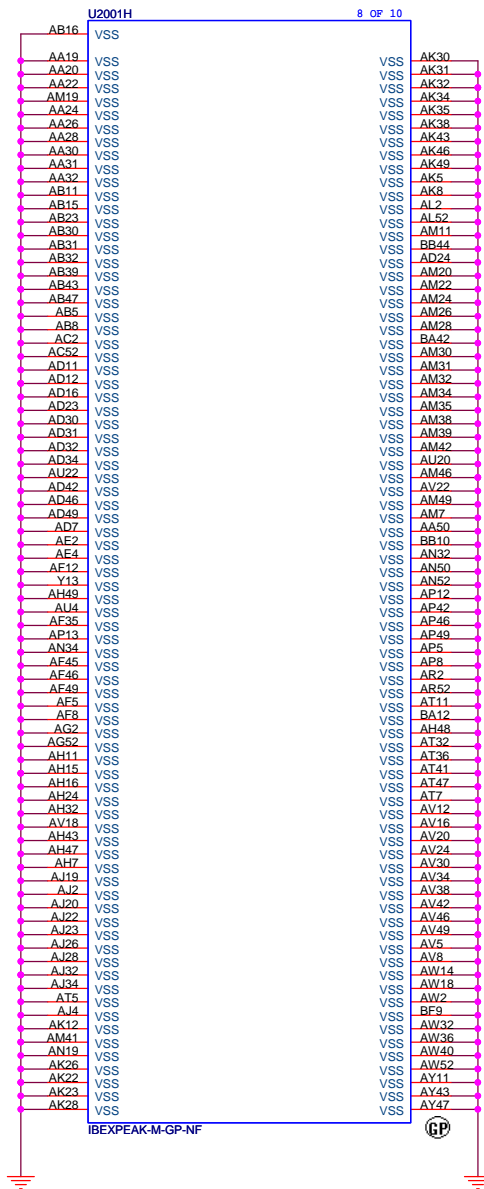
Title **PCH (SPI/RTC/LPC/SATA/IHDA)**

Size Document Number

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Rev **X00**

Vostro Calpella



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Title


(Reserve)

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Document Number

Rev

Custom

Vostro Calpella

SA


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<Core Design>



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Custom

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Vostro Calpella

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SA


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<Core Design>



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Size
A3


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Vostro Calpella

Rev
SA

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Size

Document Number

Rev

Custom

Vostro Calpella


SA

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<Core Design>



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(Reserve)

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<Core Design>



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Title


(Reserve)

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Title

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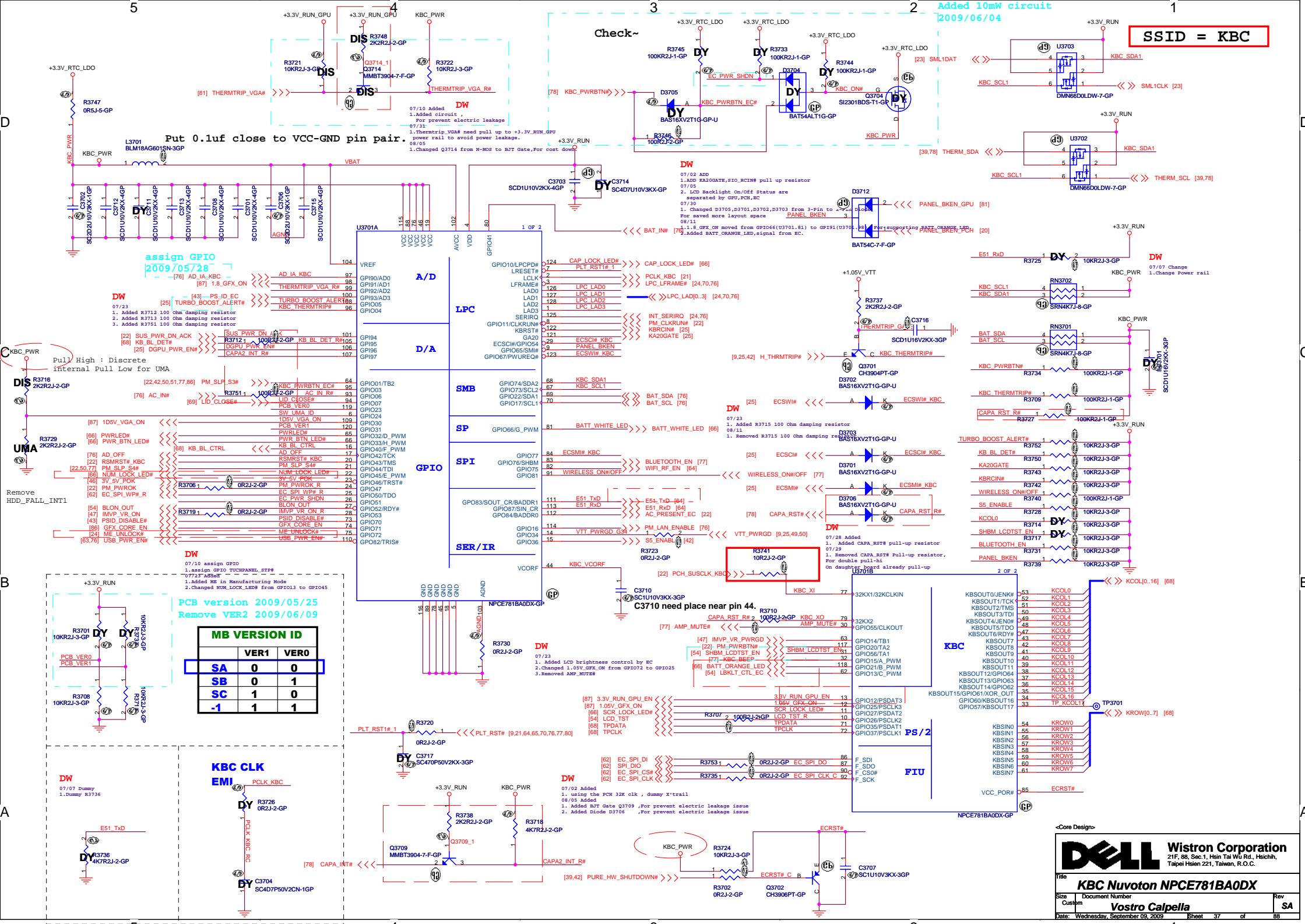
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A3

Document Number
Vostro Calpella

Date: Wednesday, September 09, 2009

Rev
SA

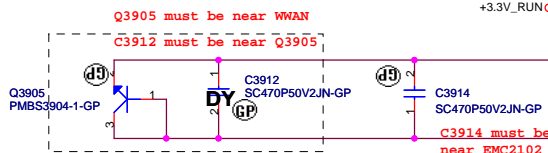
Sheet 36 of 88



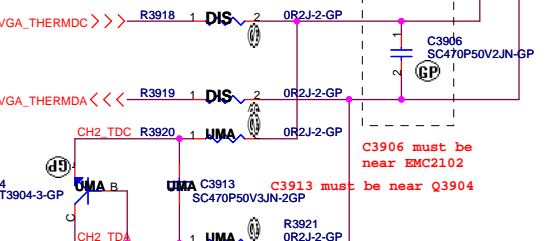
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SSID = Thermal

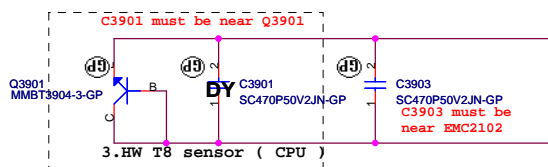
1. WWAN



2. GPU Sensor

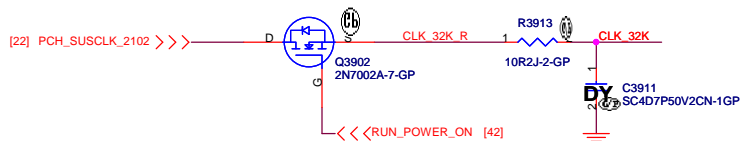


3. HW T8 sensor (CPU)



Layout notice :
Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.

32K suspend clock output



DW

07/10 Del
1. Not reserve S5 power source rail for EMC2102 ??

GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

TRIP_SET Pin Voltage
 $V_DEGREE = ((Degree - 75) / 21)$
T8 shutdown is set 88 deg-C.

DW

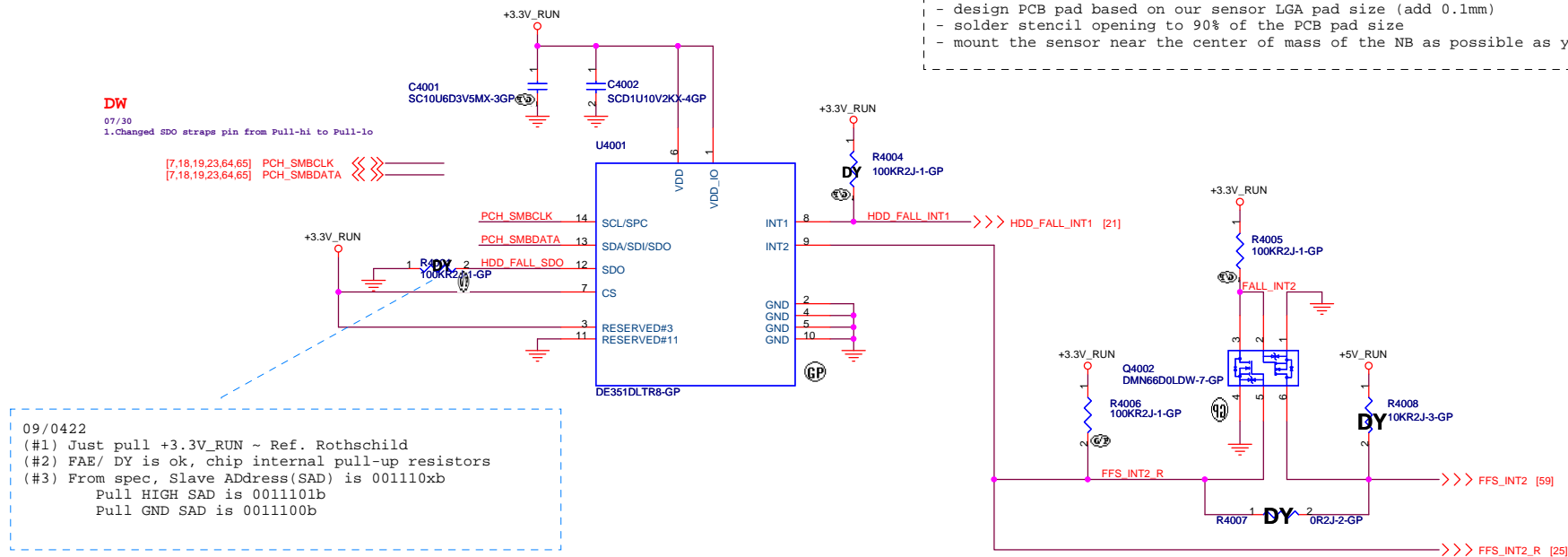
07/28 Removed
1. Removed U3902 AND gate.

<Core Design>

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Title Thermal/Fan Controllor EMC2102			
Size Custom	Document Number	Rev SA	
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SSID = User.Interface

Free Fall Sensor



Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

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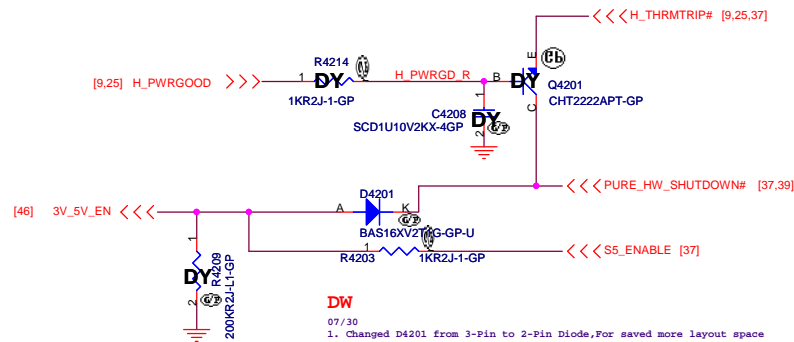
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Free Fall Sensor					
Size	Document Number			SA	
Custom	Vostro Calpella				
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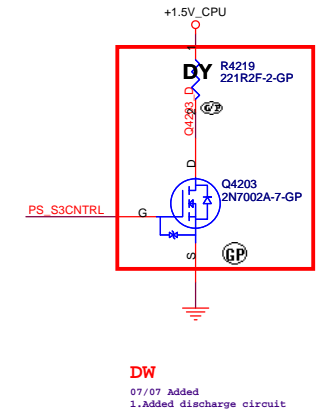
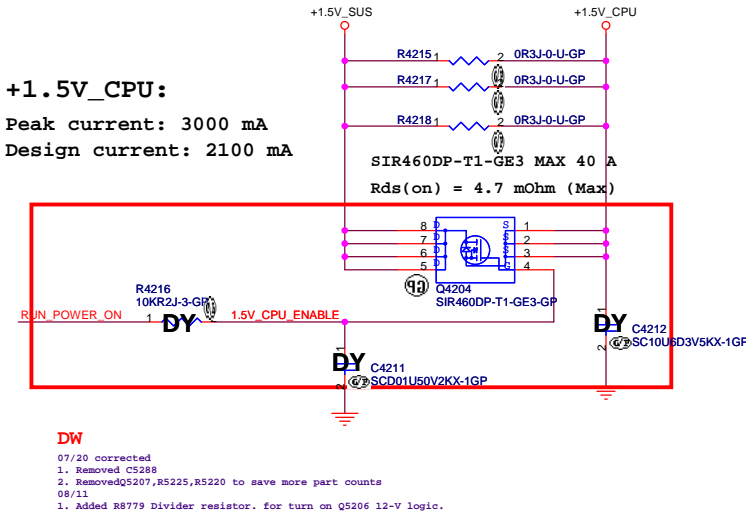
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Title			
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Size Custom	Document Number Vostro Calpella		Rev SA
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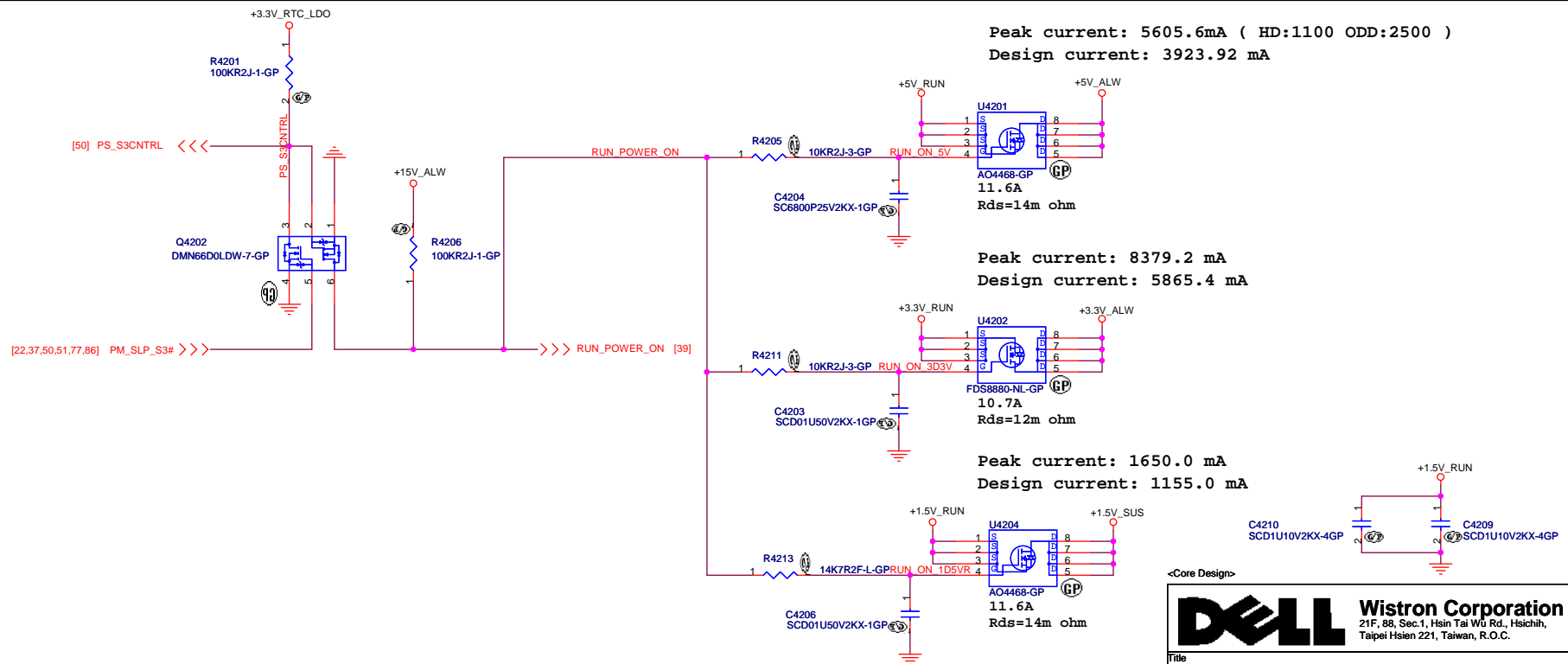
```
SSID = Reset.Suspend
```



Peak current: 3000 mA
Design current: 2100 mA



Calpella Platform S3 Power Reduction Platform
S3 Power Reduction CRB Implementation
Design Details

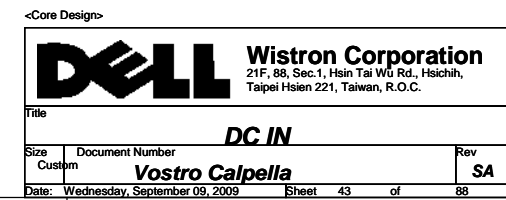


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Title			
<i>Power Plane Enable</i>			
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Title

(Reserve)

Size
A3


Document Number
Vostro Calpella

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SA

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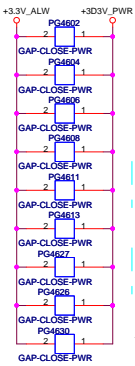
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Title

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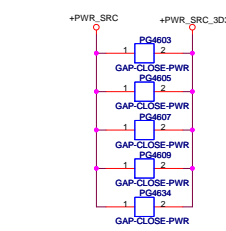
Size	Document Number	Rev
Custom	Vostro Calpella	SA

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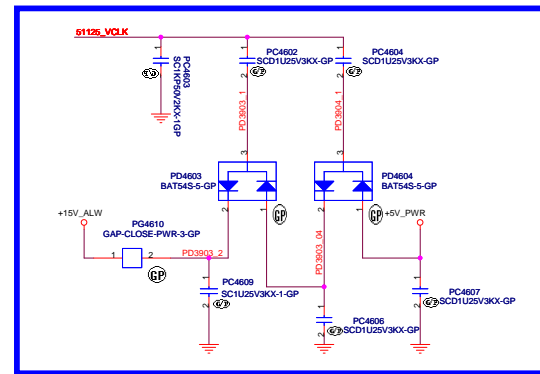
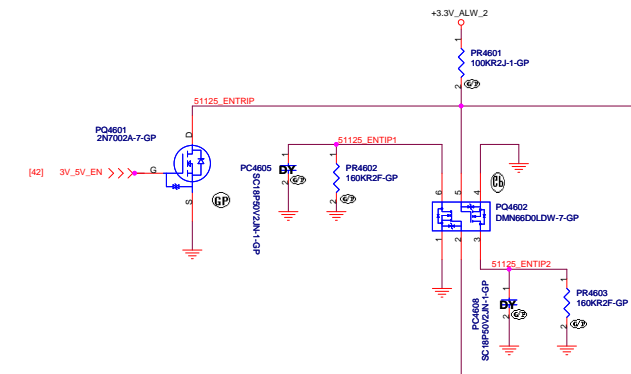
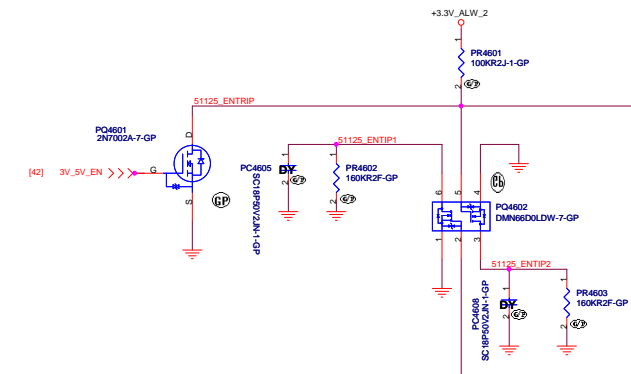
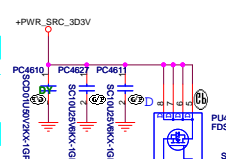


2009/08/24
UMA(Auburndale)
Design Current =7.61A
11.96A<OCP<14.13A

2009/08/24
DIS(Auburndale)
Design Current =8.23A
12.93A<OCP<15.28

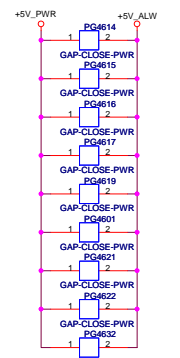
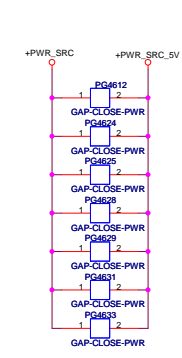


2009/08/03
UMA(Auburndale)
Design Current =8.23A
12.93A<OCP<15.28



2009/08/24
UMA(Auburndale)
Design Current =8.52A
13.38A<OCP< 15.82A

2009/08/24
DIS(Auburndale)
Design Current =8.53A
13.39A<OCP< 15.83A

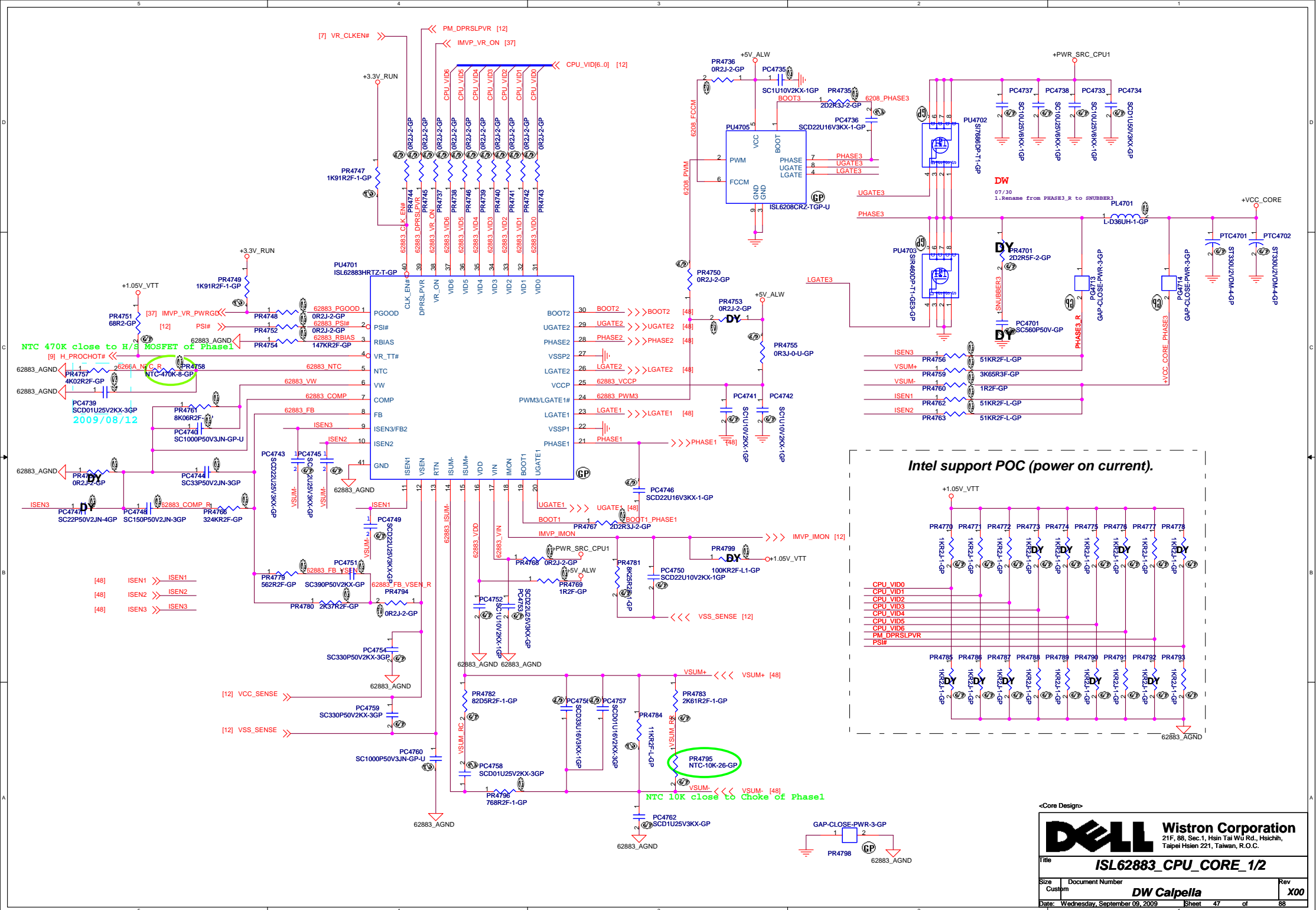


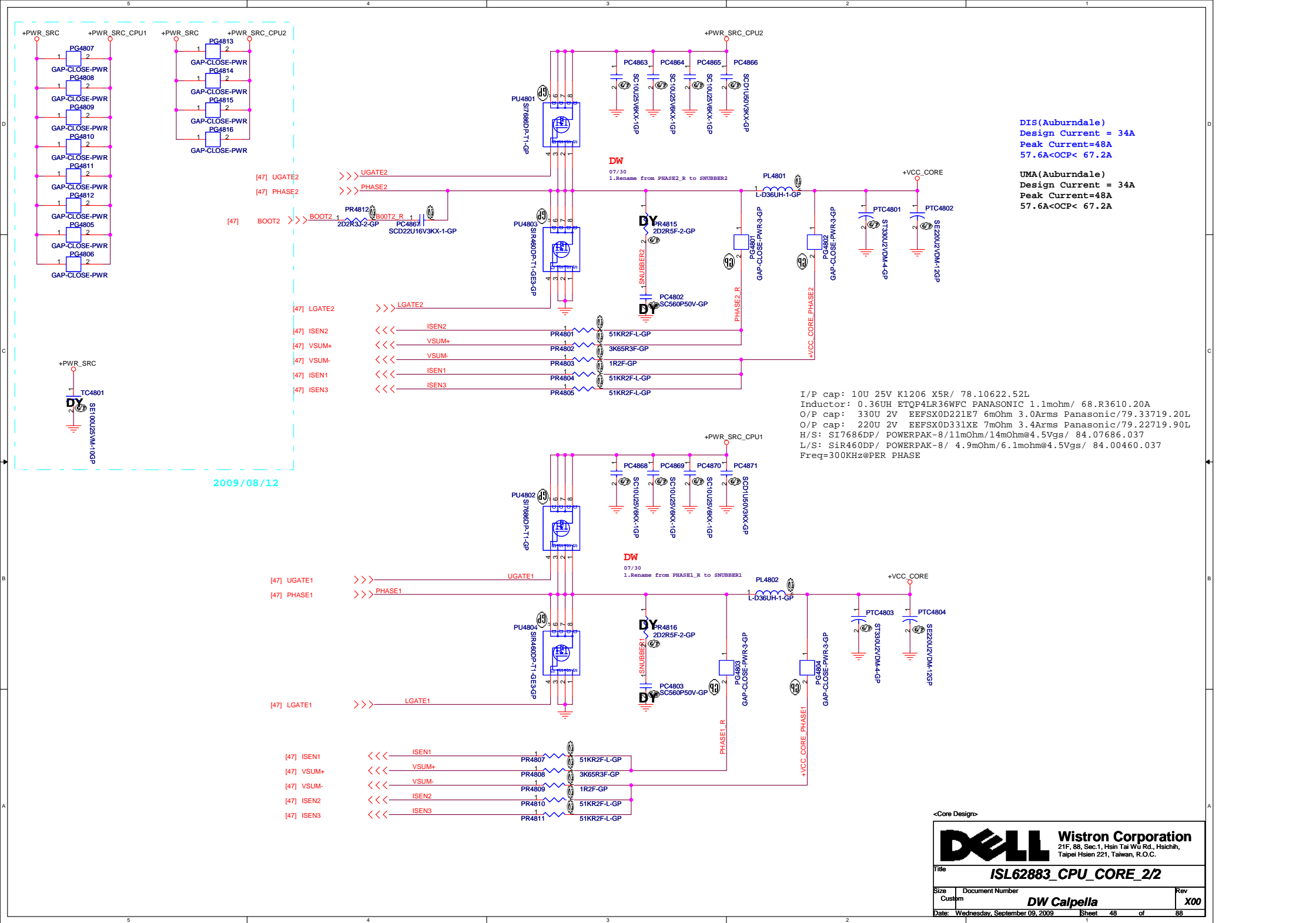
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMB104T-3R3MS Cyntec 11.8mohm Isat =16Arms 68.3R310.20C
O/P cap: 220U 6.3V PSLV0J227M(25) 25mohm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEP5LB20J107M(45) 8R 45mohm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS58884 SO-8/ 23mohm/30mohm4.5Vgs/ 84.08884.037
L/S: FDS5690AS SO-8/ 12mohm/15mohm4.5Vgs/ 84.06690.E37

TONSEL	CH1	CH2	SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
GND	200kHz	265kHz	Operating Mode	OOA Auto Skip	Auto Skip	PWM only
VREF	245kHz	305kHz				
VREG3	300kHz	375kHz				
VREG5	365kHz	460kHz				

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 20 mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 6.3V PSLV0J227M(25) 25mohm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEP5LB20J107M(45) 8R 45mohm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS58884 SO-8/ 23mohm/30mohm4.5Vgs/ 84.08884.037
L/S: FDS5690AS SO-8/ 12mohm/15mohm4.5Vgs/ 84.06690.E37





The schematic diagram illustrates the power supply section of the TMS320C6701 evaluation module. It shows the connection of various power pins to the TMS320C6701 chip. Key components include resistors PR4902, PR4903, PR4907, PR4908, and PR4909; capacitors PC4907, PC4912, and PC4908; and integrated circuits PL4901, PL4902, and PL4903. The diagram is divided into two main sections: the top section for the TMS320C6701 chip and the bottom section for the TMS320C6701 chip. The top section shows the connection of VTT_PWRGD, VTT_PWRGD, and VTT_PWRGD to the TMS320C6701 chip. The bottom section shows the connection of VTT_PWRGD, VTT_PWRGD, and VTT_PWRGD to the TMS320C6701 chip.

```
Frequency setting
470K  -->290KHz
200K  -->340KHz
100K  -->380KHz
 39K  -->430KHz
```

2009/08/24

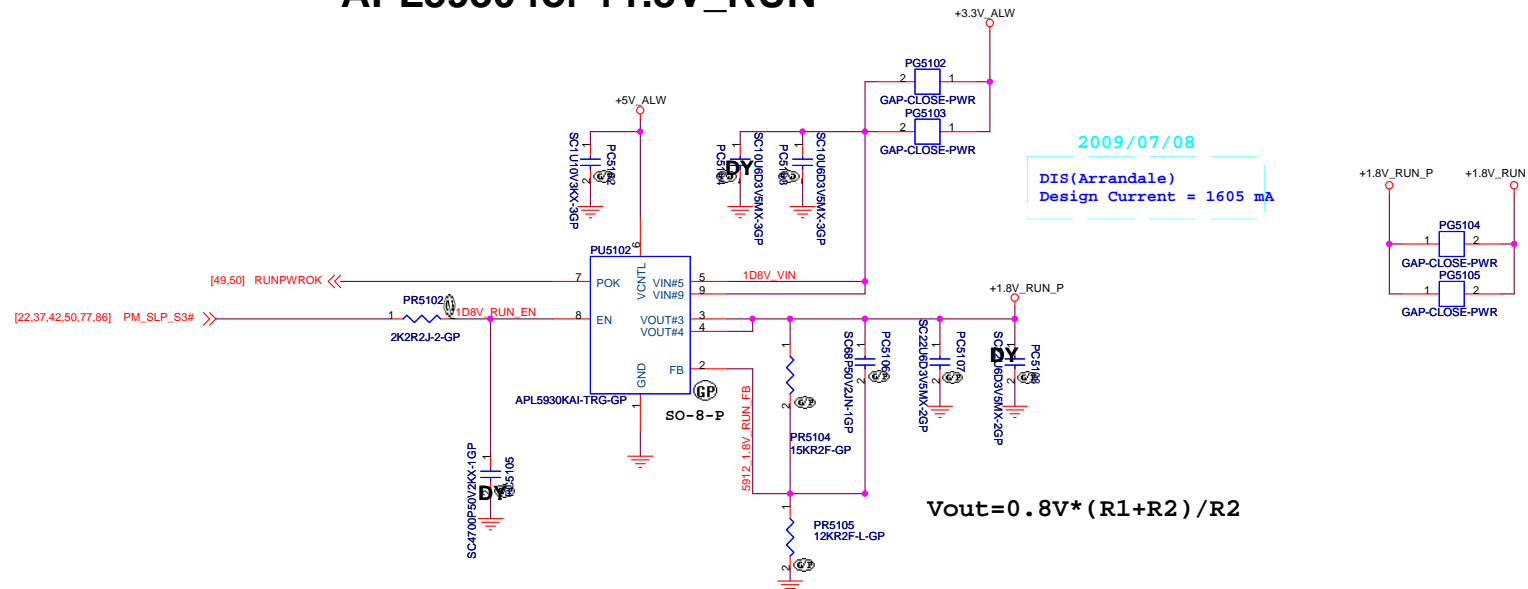
2009/08/24

2009/08/05

$$V_{out} = 0.704V * (R1 + R2) / R2$$


```
SSID = PWR.Plane.Regulator_1p8v
```

APL5930 for +1.8V_RUN


$$V_{out} = 0.8V * (R1 + R2) / R2$$

2009/07/08

DIS(Arrandale)
Design Current = 1605 mA




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Title			
APL5930 +1.8V RUN			
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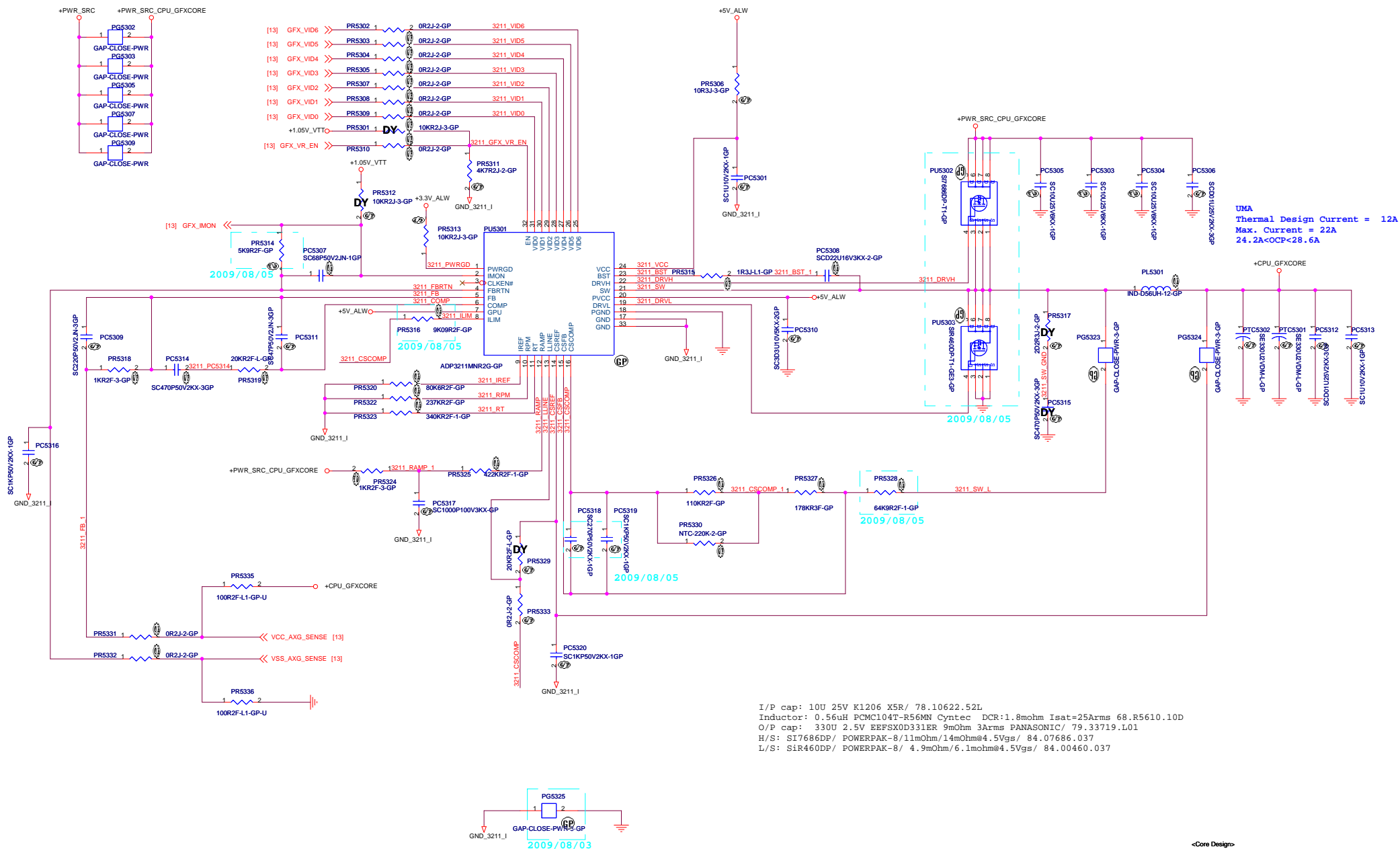
Title

(Reserve)

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```
SSID = CPU.GFX.Regulator
```



I/P cap: 10U 25V KI206 X5R/ 78.10622.52L
 Inductor: 0.56uH PCMC104T-R56Mn Cymtec DCR:1.8mohm Isat=25Arms 68.R5610.10D
 O/P cap: 330U 2.5V EEFS04D331ER 9ymohm 3Arms PANASONIC/ 79.33719.L01
 L/S: S17686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
 H/S: SIR4660DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

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Title				ADP3211 CPU GFXCORE			
Size	Custom	Document Number				Rev	X00
		DW Calpella UMA					
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SSID = VIDEO

Close PCH

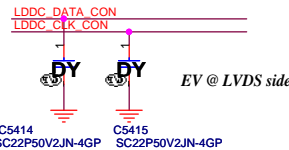
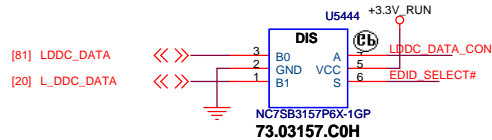
Close GPU

DW

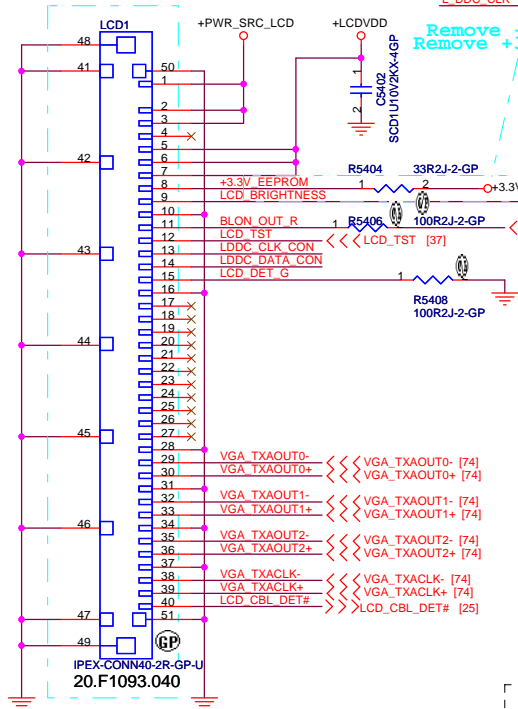
07/07 Added
1. Added LVDS DDC CLK/DAT Pull Hi

UMA/DIS LVDS DDC CLK/DAT select circuit

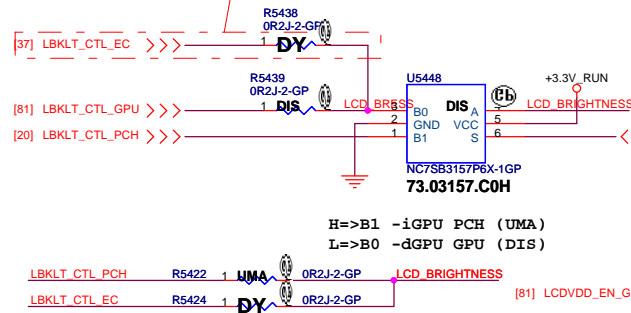
H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)



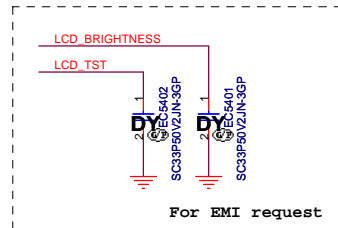
LVDS CONNECTOR



UMA/DIS LVDS PWM select circuit



2009/06/19



DW

07/30
1. Changed D5407 from 3-Pin to 2-Pin Diode, For saved more layout space

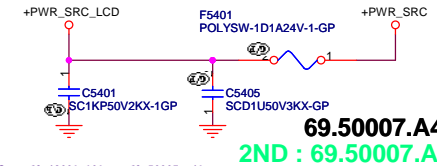
SSID = Inverter

INVERTER POWER

DW

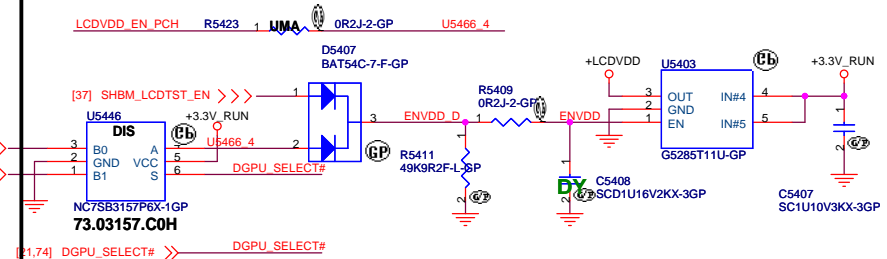
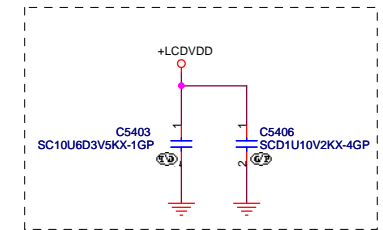
08/18
1. Changed F5401 P/N from 69.43001.101 to 69.50007.A41,
For new projects need changed panel PWRSRC use poly-fuse instead of fuse.

69.50007.A41
2ND : 69.50007.A31



SSID = VIDEO

LCD POWER



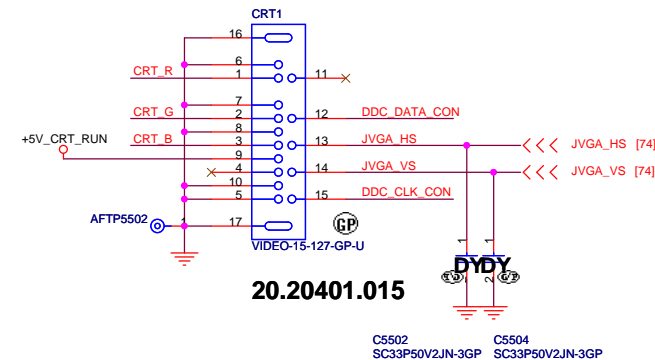
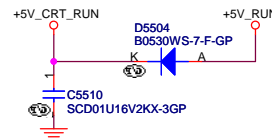
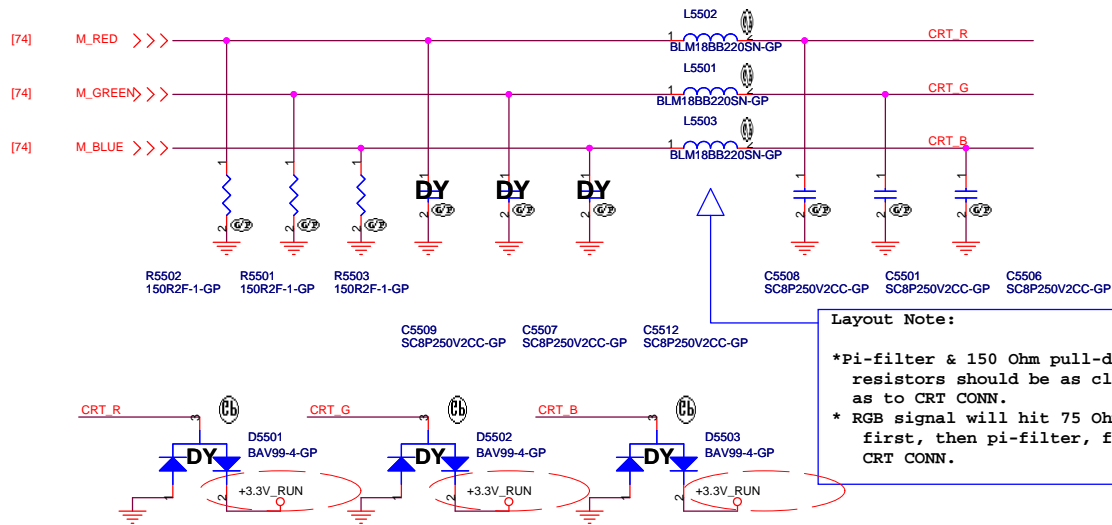
H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title			Rev
LCD/Inverter Connector			SA
Size	Document Number		
Custom	Vostro Calpella		
Date	Wednesday, September 09, 2009	Sheet	54 of 88

SSID = VIDEO



DW

07/14 Change

1.Change CRT1 CONN PN from 20.20431.015 to 20.20401.015 base on ME emm files.

AFTP5503 1 +5V_CRT_RUN

AFTP5501 1 DDC DATA CON

AFTP5509 1 DDC CLK CON

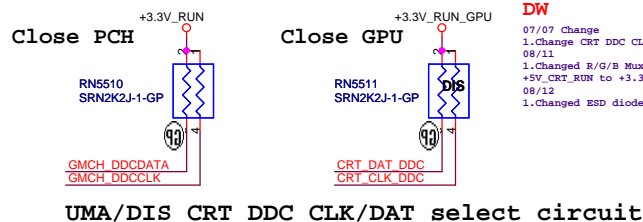
AFTP5507 1 CRT_R

AFTP5506 1 CRT_G

AFTP5508 1 CRT_B

AFTP5504 1 JVGA_HS

AFTP5505 1 JVGA_VS



DW

07/07 Change

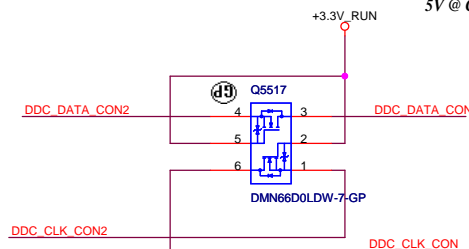
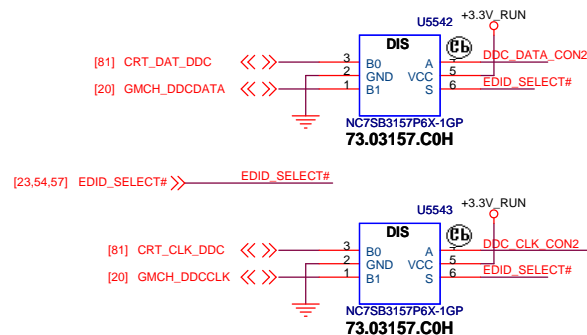
1.Change CRT DDC CLK/DAT Circuit

08/11

1.Changed R/G/B Mux,ESD diode power rail from +5V_CRT_RUN to +3.3V_RUN_GPU for correct.

08/12

1.Changed ESD diode power rail from +3.3V_RUN_GPU to +3.3V_RUN for power header.



H=>B1 -iGPU PCH (UMA)


L=>B0 -dGPU GPU (DIS)

GMCH_DDCDATA R5593 1 UMA 0R2J-2-GP DDC_DATA_CON2

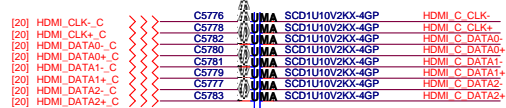
GMCH_DDCCLK R5592 1 UMA 0R2J-2-GP DDC_CLK_CON2

(Blank)

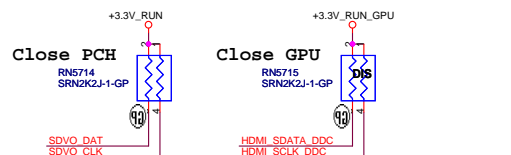
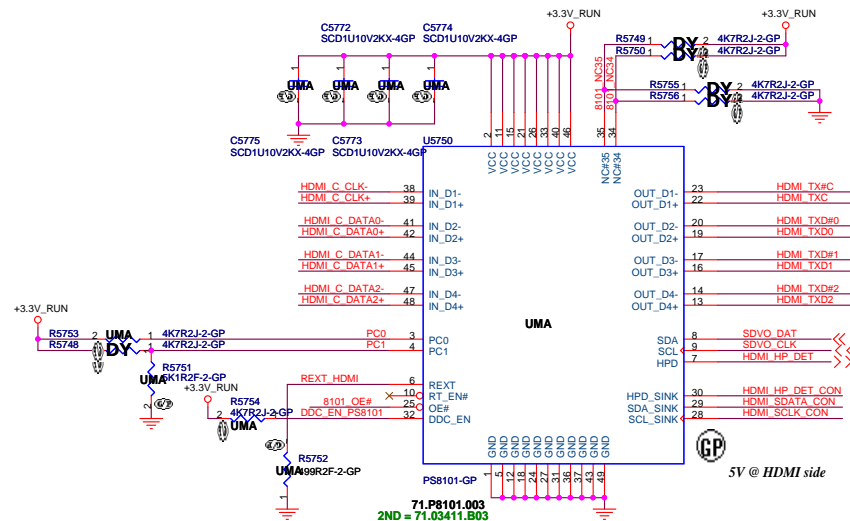
<Core Design>

		Wistron Corporation	
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Title			
(Reserve)			
Size Custom	Document Number Vostro Calpella		Rev SA
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[81]	IFPC_D2+	>>>	C5769	DIS1	SCDU1U10V2KX-4GP	HDMI TXD2
[81]	IFPC_D2-	>>>	C5764	DIS1	SCDU1U10V2KX-4GP	HDMI TXD#2
[81]	IFPC_D1+	>>>	C5770	DIS1	SCDU1U10V2KX-4GP	HDMI TXD1
[81]	IFPC_D1-	>>>	C5765	DIS1	SCDU1U10V2KX-4GP	HDMI TXD#1
[81]	IFPC_D0+	>>>	C5768	DIS1	SCDU1U10V2KX-4GP	HDMI TXD0
[81]	IFPC_D0-	>>>	C5767	DIS1	SCDU1U10V2KX-4GP	HDMI TXD#0
[81]	IFPC_TXC+	>>>	C5771	DIS1	SCDU1U10V2KX-4GP	HDMI TXC
[81]	IFPC_TXC-	>>>	C5766	DIS1	SCDU1U10V2KX-4GP	HDMI TX#C



UMA HDMI level shift circuit



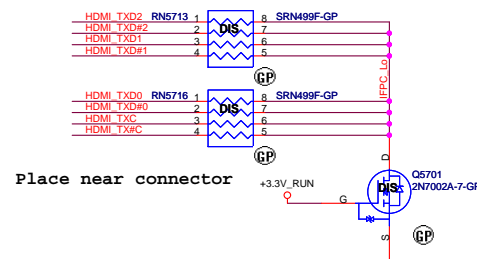
Two circuit diagrams showing the connection of the NC7S157P6X-1GP (73.03157.C0H) to the HDMI0 block.

Top Diagram (HDMI_SDATA_DDC):

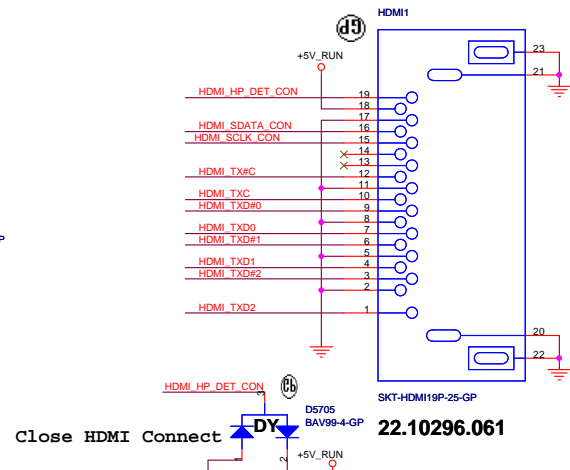
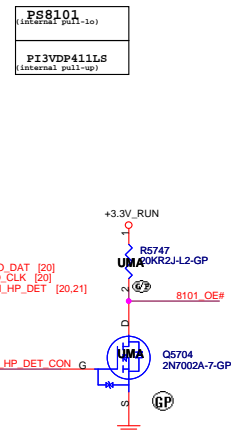
- Chip: NC7S157P6X-1GP (73.03157.C0H)
- Pin 1 (B0): GND
- Pin 2 (B1): GND
- Pin 3 (A): HDMI_SDATA_DDC << (via R5771 0R2J-2-GP)
- Pin 4 (A): +3.3V RUN
- Pin 5 (B): HDMI_SCLCK_CON_L (via R5746 0R2J-2-GP)
- Pin 6 (B): EDID_SELECT#

Bottom Diagram (HDMI_SCLCK_CON_L):

- Chip: NC7S157P6X-1GP (73.03157.C0H)
- Pin 1 (B0): GND
- Pin 2 (B1): GND
- Pin 3 (A): HDMI_SCLCK_CON_L << (via R5772 0R2J-2-GP)
- Pin 4 (A): +3.3V RUN
- Pin 5 (B): HDMI_SCLCK_CON_L (via R5747 0R2J-2-GP)
- Pin 6 (B): EDID_SELECT#



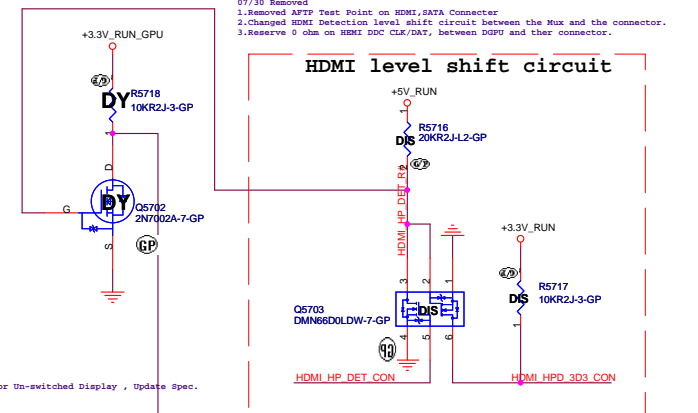
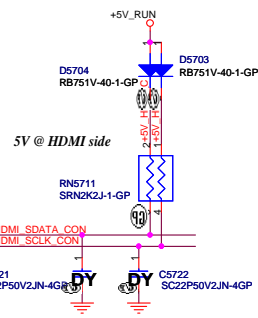
jitter elimination control



DW

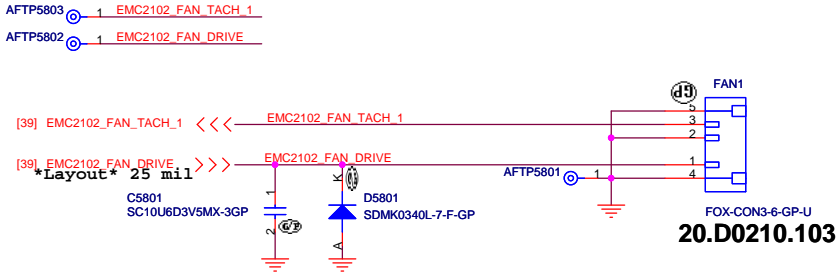
07/30 Removed

- 1.Removed AFTP Test Point on HDMI,SATA Connector
- 2.Changed HDMI Detection level shift circuit between the Mux and the connector.
- 3.Reserve 0 ohm on HEMI DDC CLK/DAT, between DGPU and ther connector.

[illegible]

SSID = Thermal

Fan Connector



<Core Design>



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Title

FANSize
A3

Document Number

Vostro Calpella

Rev

SA

Date: Wednesday, September 09, 2009

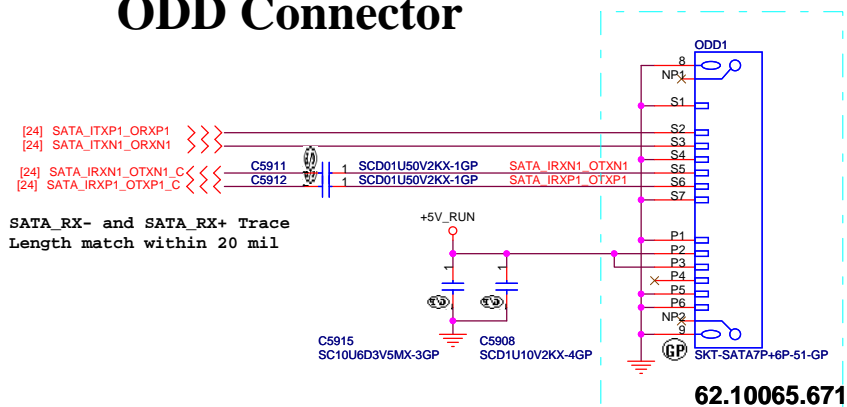
Sheet 58

88

SSID = SATA

SSID = SATA

ODD Connector



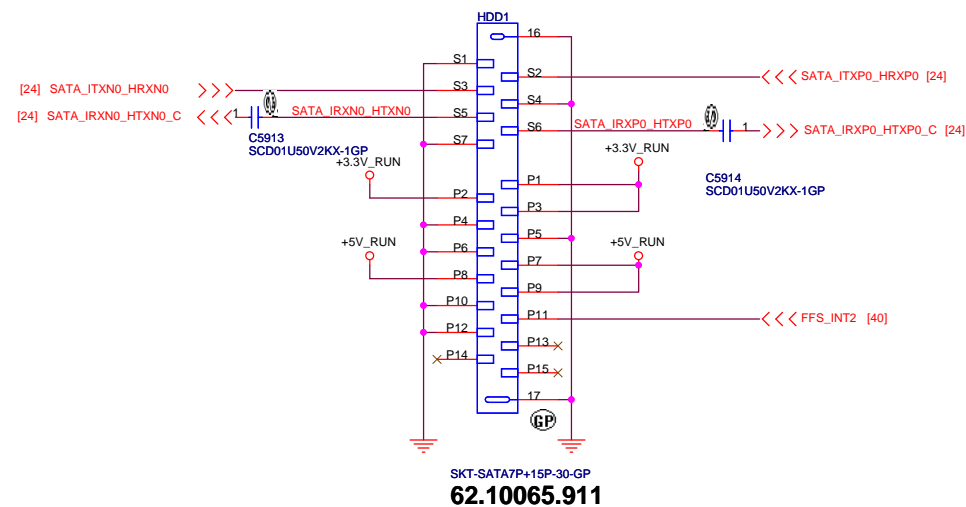
SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

CONN change
2009/05/25
2009/07/23

DW

07/30 Removed
1. Removed AFTP Test Point on HDMI, SATA Connector

SATA HDD Connector

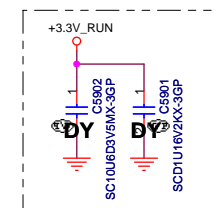
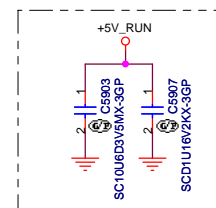


Close to CONN
5V power pin

Close to CONN
3.3V power pin

DW

07/30 Removed
1. Removed AFTP Test Point on HDMI, SATA Connector



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Title		
HDD/ODD Connector		
Size A3	Document Number Vostro Calpella	Rev SA
Date: Wednesday, September 09, 2009		
Sheet 59 of 88		

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<Core Design>

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Title

(Reserve)

Size

Custom

Document Number

Vostro Calpella

Rev


SA

Date: Wednesday, September 09, 2009

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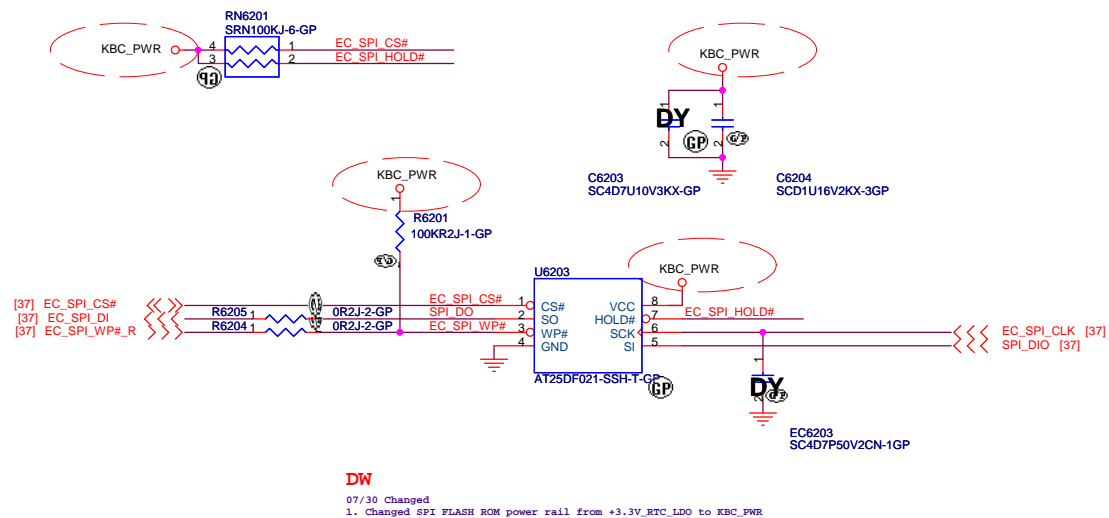
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<Core Design>

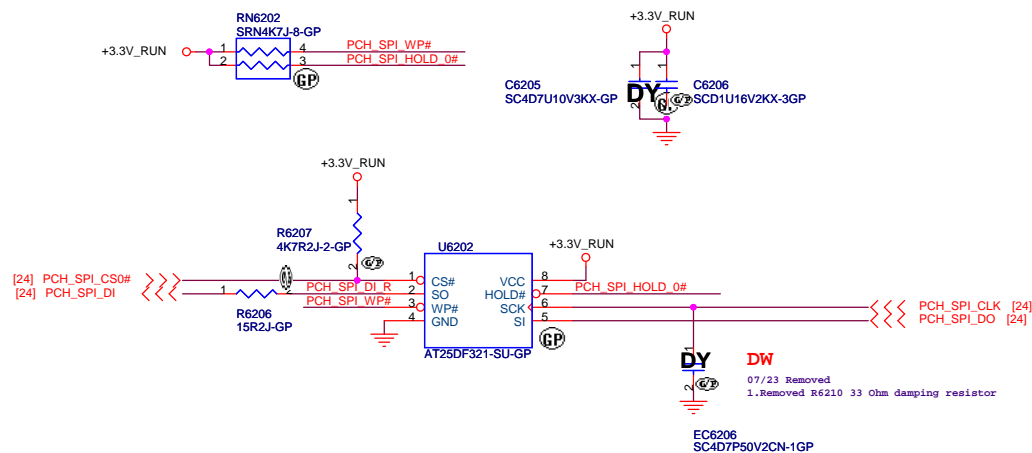
		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
(Reserve)			
Size Custom	Document Number Vostro Calpella		Rev SA
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SSID = Flash.ROM

SPI FLASH ROM (256K bytes) for KBC

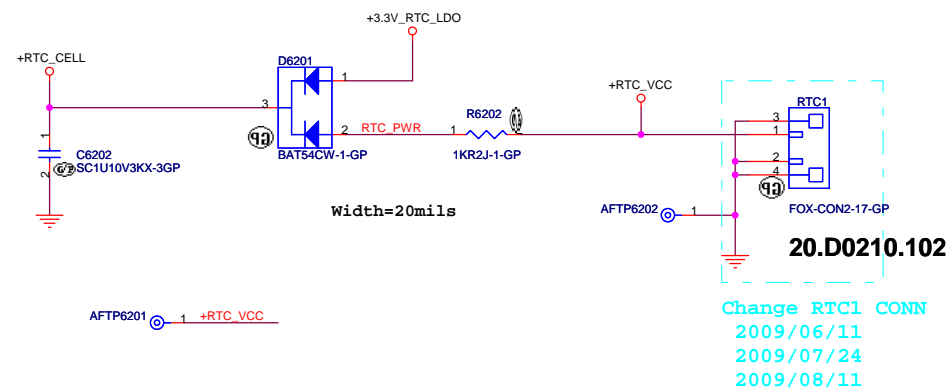


SPI FLASH ROM (4M bytes) for PCH



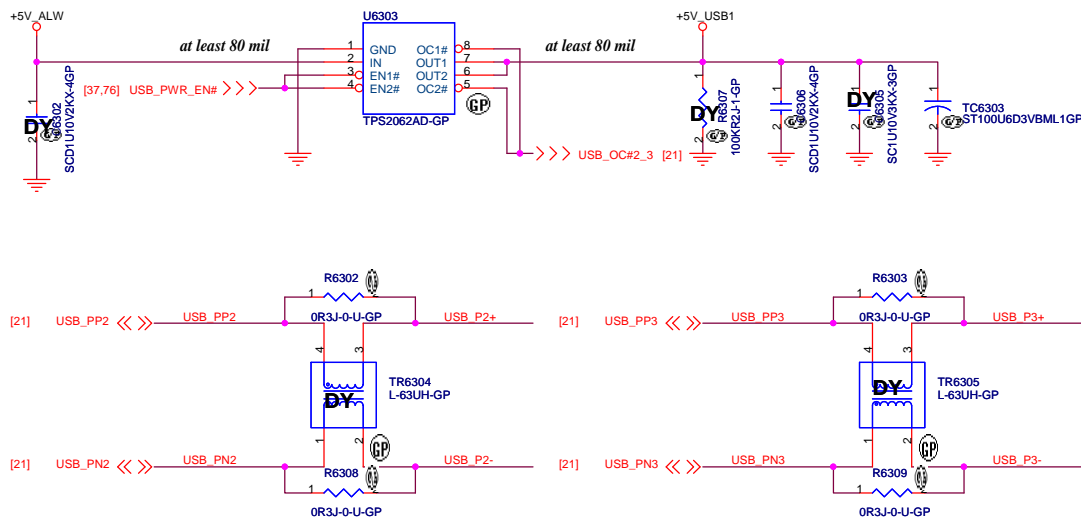
SSID = RBATT

RTC Connector



SSID = USB

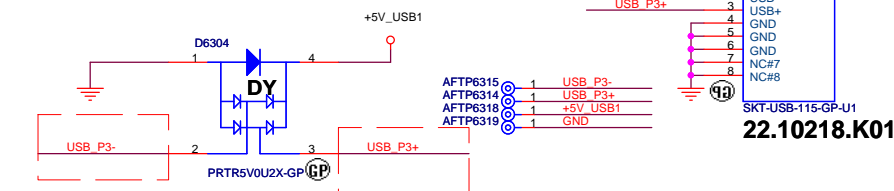
USB Power



DW

07/29

1.Changed USB ESD Protection Diode between the common mode choke and the USB connector data pins



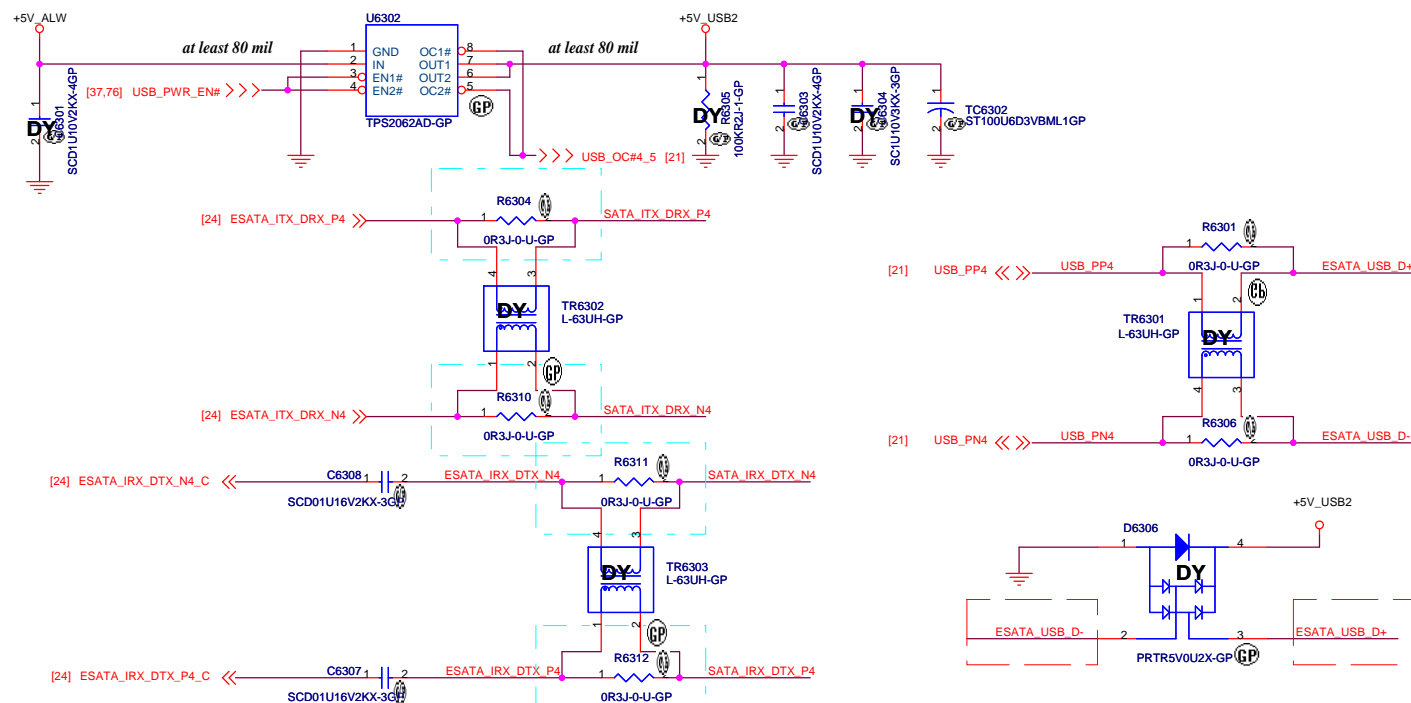
DW

07/14 Change

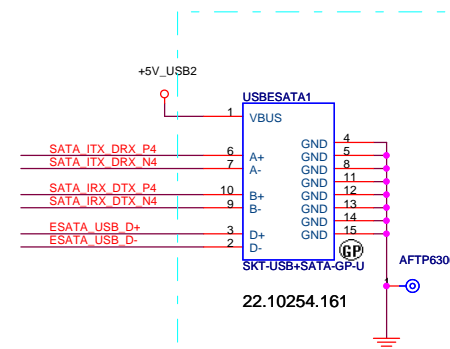
1.Change USB2,USB3 CONN PN from 22.10321.001 to 22.10218.731 base on ME emm files.

Change CONN 2009/05/27
2009/07/23

ESATA Power



Change to 0603 size 2009/06/08



Change CONN 2009/05/27

DW

07/30 Removed

1.Removed AFTP Test Point on HDMI,SATA Connector



<Core Design>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
USB /ESATA Port					
Size	Document Number				Rev
Custom	Vostro Calpella				SA
Date:	Wednesday, September 09, 2009	Sheet	63	of	88

SSID = Wireless

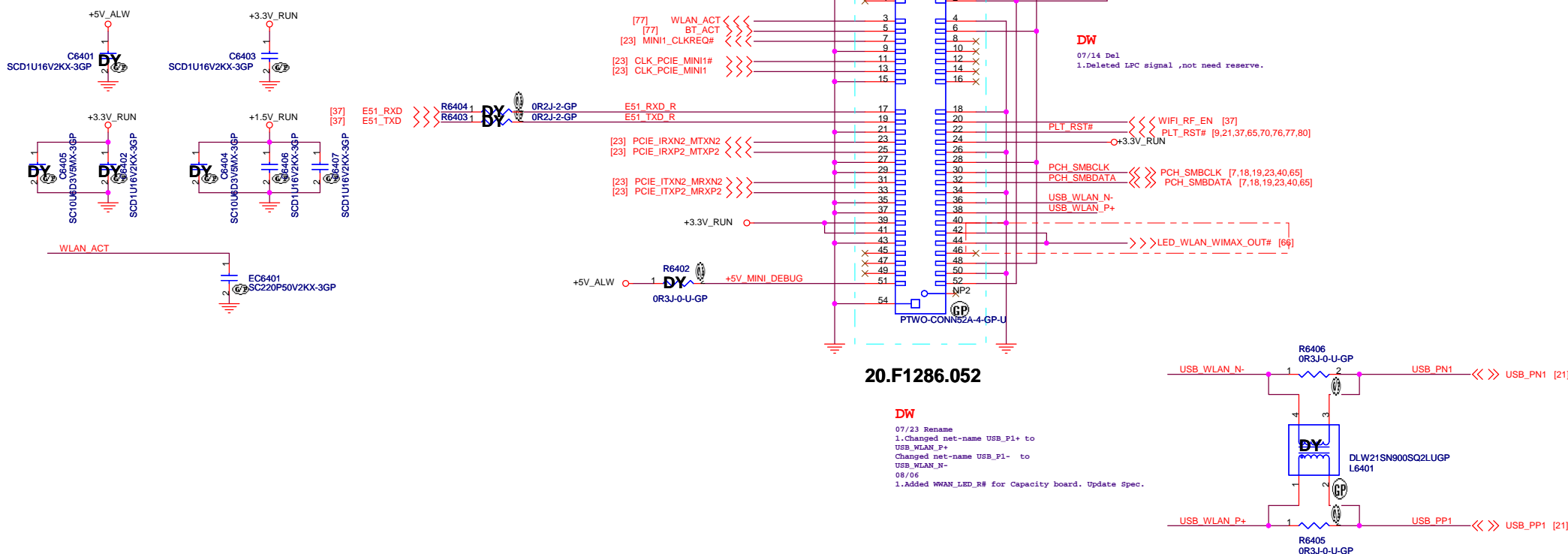
Mini Card Connector(802.11a/b/g/n)

Change CONN

2009/05/25

2009/06/11

2009/07/23



20.F1286.052

DW

07/23 Rename
1.Changed net-name USB_P1+ to
USB_WLAN_P+
Changed net-name USB_P1- to
USB_WLAN_N-
08/06
1.Added WLAN_LED_R# for Capacity board. Update Spec.

<Core Design>



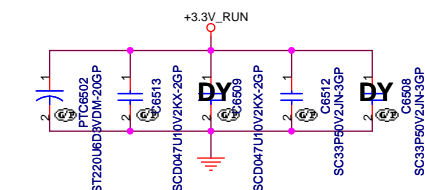
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title MINICARD(WLAN)/ITP CONN		
Size A3	Document Number Vostro Calpella	Rev SA
Date: Wednesday, September 09, 2009	Sheet 64 of 88	

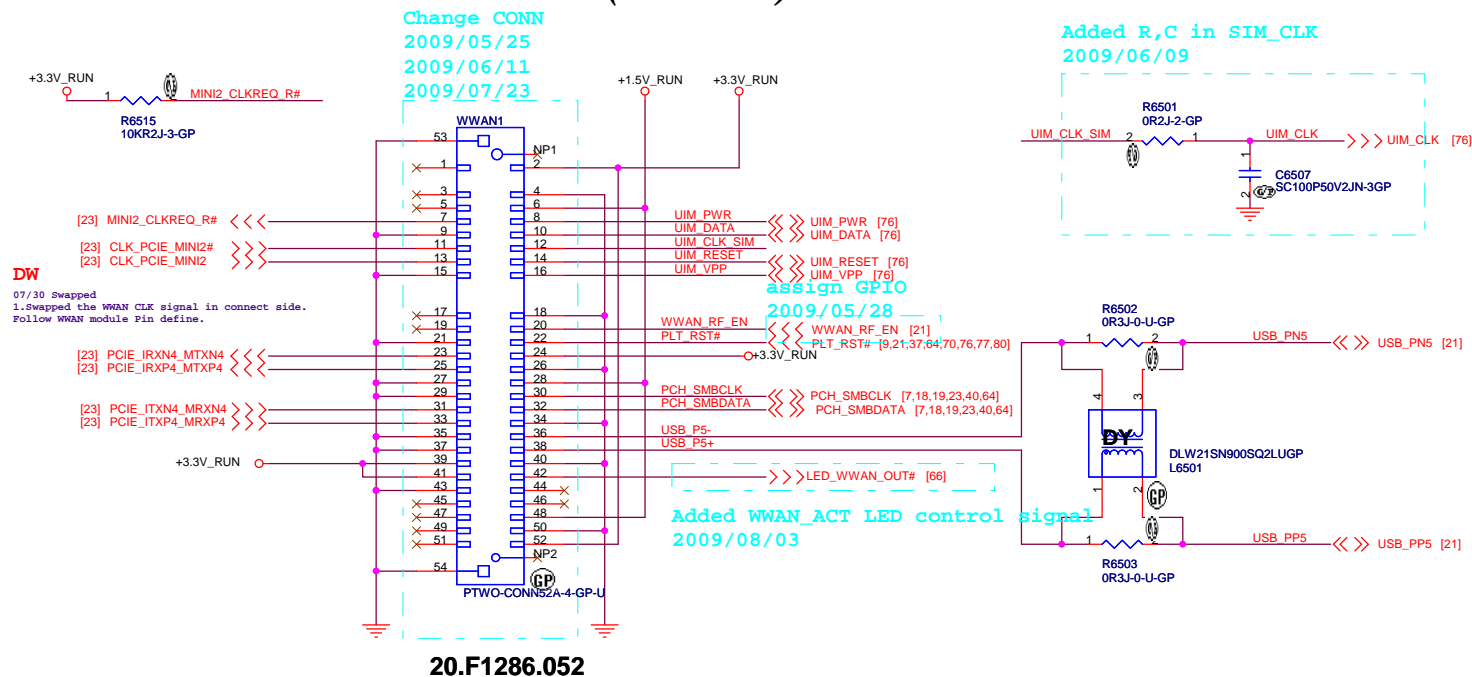
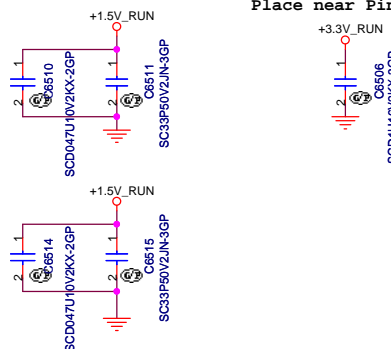
SSID = Wireless

Mini Card Connector(WWAN)

Place near MINI Card CONN



Place near Pin 24



<Core Design>



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Title

WWAN Connector

Size
A3

Document Number

Vostro Calpella

Rev

SA

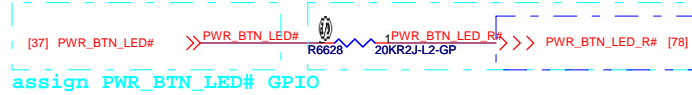
Date: Wednesday, September 09, 2009

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For LED & Capacity board:

LED Type	Color	Power rail
SCRL LED	White	ALW
CAP LED	White	ALW
NUM LED	White	ALW
PWR BTN LED	White	ALW
SATA ACT LED1	White	RUN
BT ACT LED	White	RUN
WWAN ACT LED	White	RUN
WLAN WIMAX LED	White	RUN

PWR BTN LED



For LED & Capacity board

Added PWR_BTN_LED#
2009/06/04

assign PWR_BTN_LED# GPIO

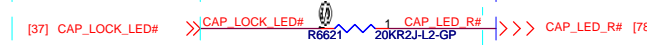
2009/06/09

SCRLK LED



For LED & Capacity board:

CAPS LED



NUM LED



Remove BJT to daughter board
2009 06/01

assign GPIO
2009/05/28

Bluetooth LED

For LED & Capacity board:



DW
08/12
1. Changed WWAN LED & WLAN WIMAX_LED . for Capacity board. Update Spec.

For IO board

LED Type	Color	Power rail
PWR LED2	White(Multi-color)	ALW
BATTERY LED2	Amber(Multi-color)	ALW
	White(Multi-color)	ALW

WWAN LED



For LED&Capacity board:

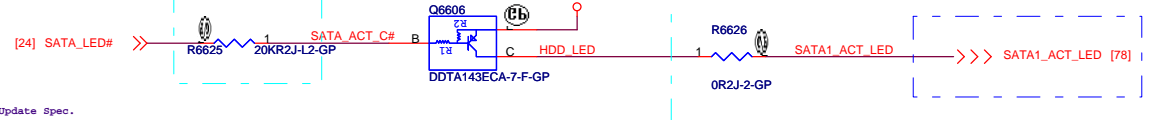
WLAN WIMAX_LED



For LED&Capacity board:

2009/06/09
2009/07/28

HD LED

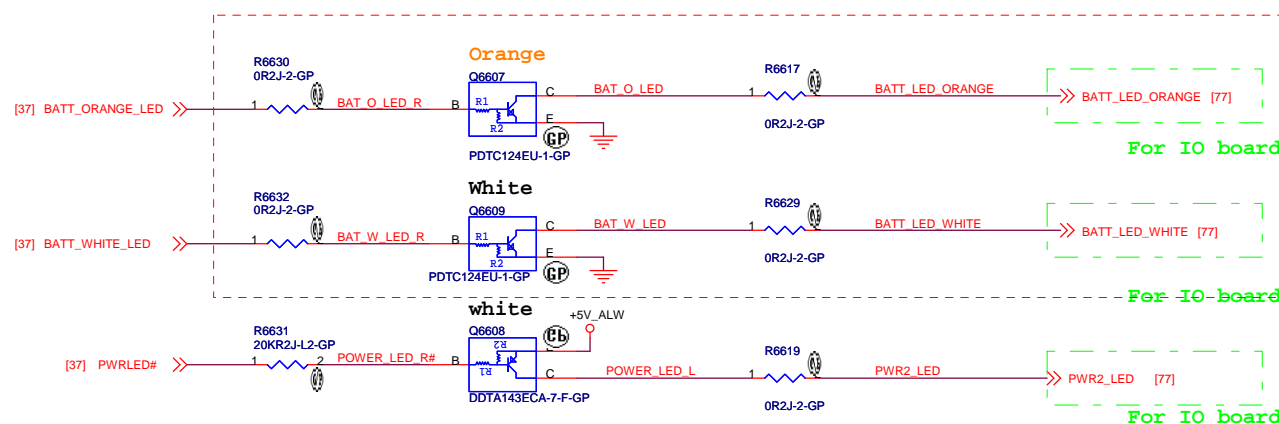


DW
07/29
1. Removed SATA2_ACT_LED from I/O board connector.

DW
07/28
1. Update R6625 from 10k to 20k ohm
08/05
1. Added WWAN_LED_R#, WLAN_LED_R# for Capacity board. Update Spec.
08/11
2. Removed BAT1_LED from Capacity board. Update Spec.

DW
07/28
1. Change Power & Battery LED from common-cathode to common-anode
08/11
1. Modified LED circuitry
08/11
1. Changed battery LED be one LED with bi-color (white and amber). for Capacity board. Update Spec.

Battery & Power LED



For IO board

For IO-board


For IO board

<Core Design>

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		Title <h1>LED</h1>	
Size A3	Document Number Vostro Calpella	Rev SA	Date: Wednesday, September 09, 2009
Sheet 66 of 88		1	

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<Core Design>



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Title

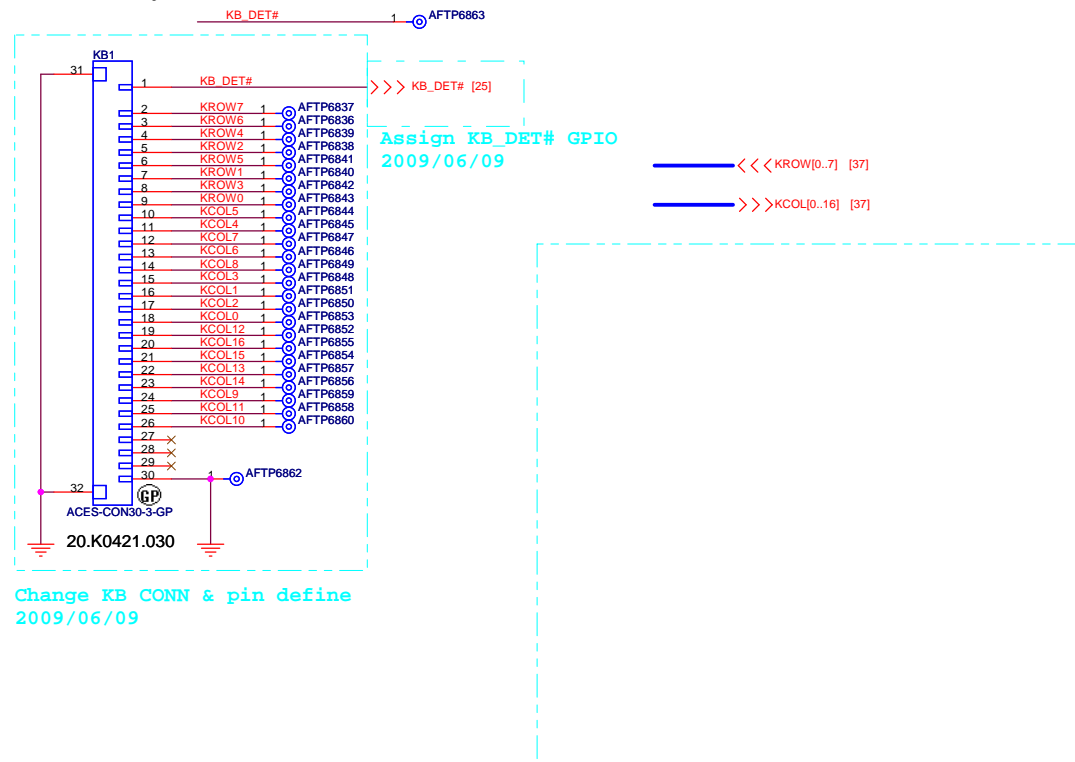
(Reserve)

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SSID = KBC

Internal KeyBoard Connector

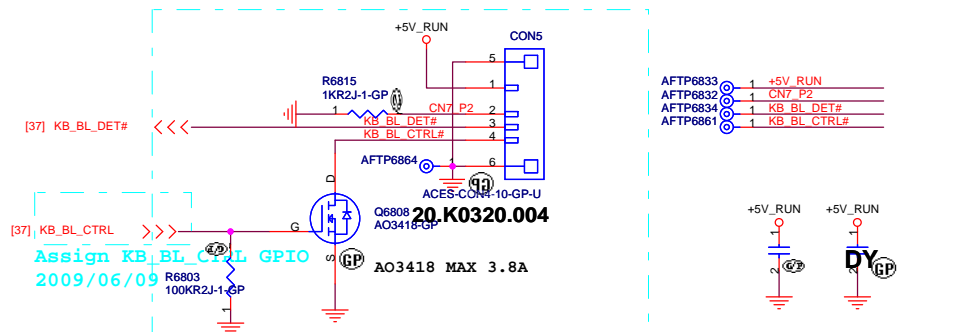


Change KB CONN & pin define
2009/06/09

Added KB1 EMI Cap
2009/06/17

DW
07/27 Removed
1.Removed KB1 EMI Cap

KB Backlight CONN

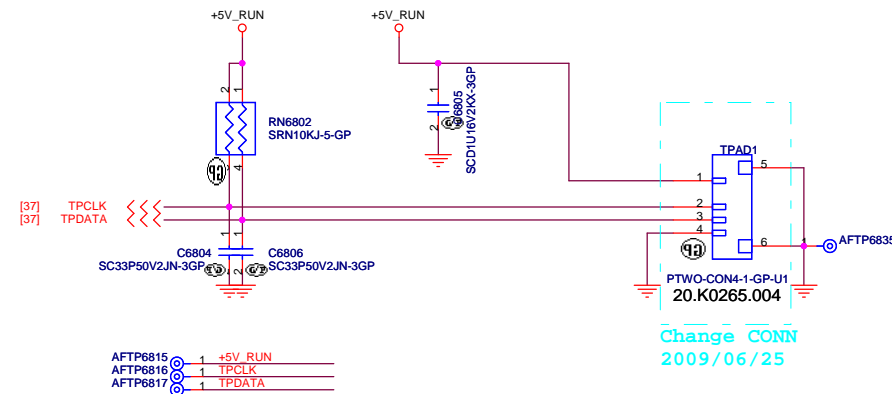


Added KB Backlight CONN
2009/06/08

Modified CONN7 pin define & added N-MOS
2009/06/09

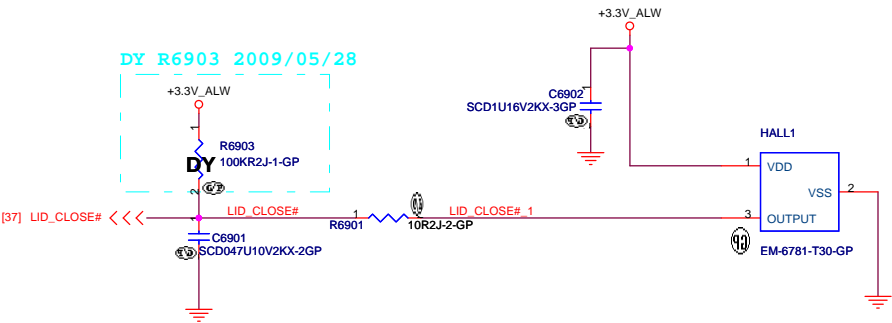
SSID = Touch.Pad

TouchPad Connector

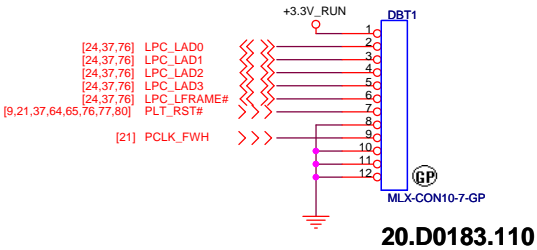


<Core Design>

Hall Sensor Connector




GOLDEN FINGER FOR DEBUG BOARD



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<Core Design>



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Title

(Reserve)

Size
Custom

Document Number
Vostro Calpella

Rev
SA

Date: **Wednesday, September 09, 2009**

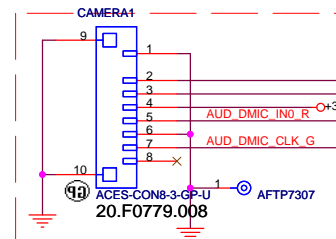
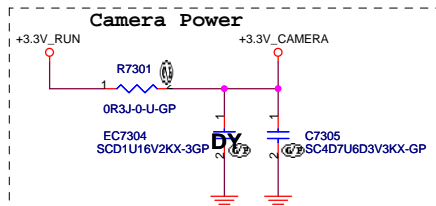
Sheet **72** of **88**

SSID = User.Interface

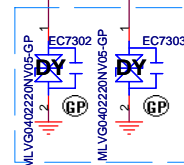
DW

07/23 Reversal
1.CAMERA1 signal Reversal
(8 -> Detect , 7 -> Gnd , ...1 -> Gnd , 2 -> USB_D+)
07/27
1.Reversal Pin 6 <-> 7 , For Cable Pin define

Camera Connector

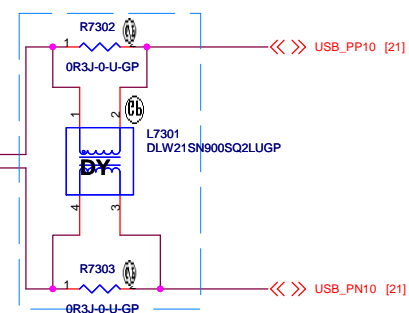


AFTP7302 1 AUD_DMIC_CLK_G
AFTP7303 1 AUD_DMIC_IN0_R
AFTP7304 1 +3.3V_CAMERA
AFTP7305 1 CAMERA_USB1-
AFTP7306 1 CAMERA_USB1+



For ESD

For EMI



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Title

Camera CONN

Size
A3

Document Number

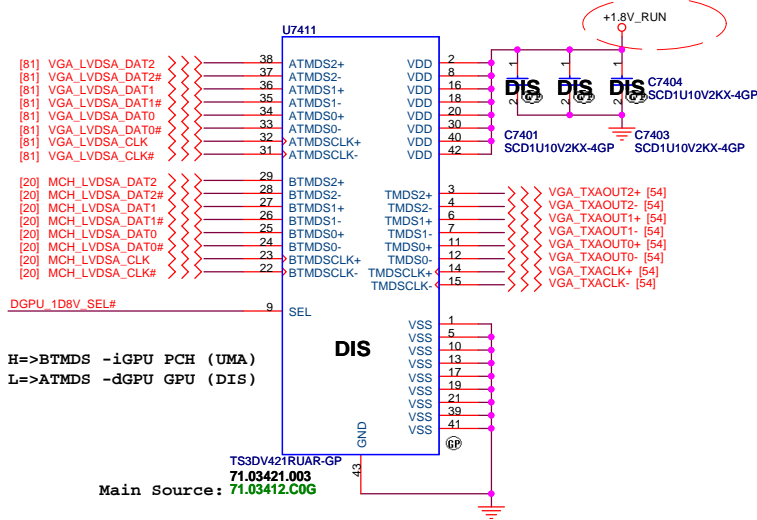
Vostro Montevina Discrete

Rev
SA

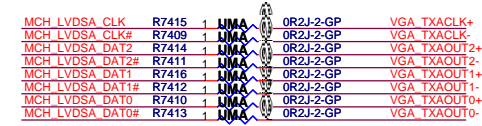
Date: Wednesday, September 09, 2009

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UMA/DIS LVDS signal select circuit



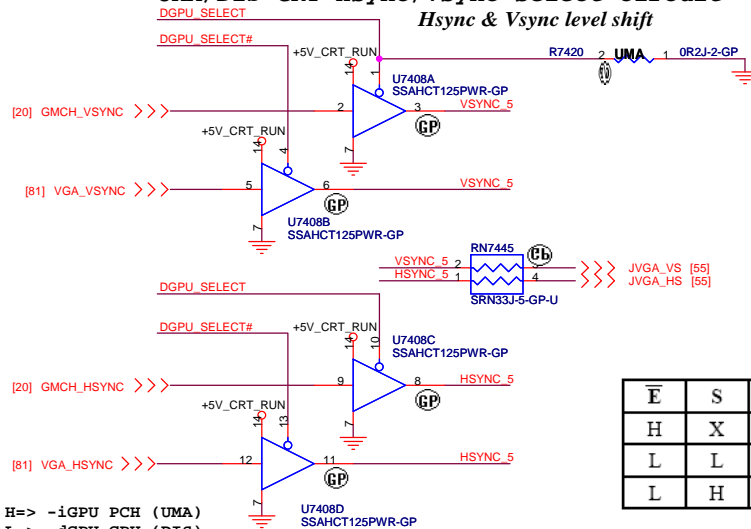
UMA LVDS signal circuit



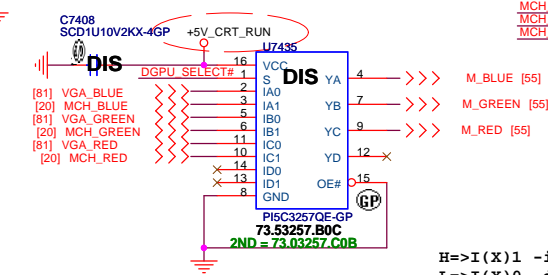
FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

UMA/DIS CRT Hsync/Vsync select circuit



UMA/DIS CRT signal select circuit



H=>I(X)1 -iGPU PCH (UMA)
L=>I(X)0 -dGPU GPU (DIS)


\bar{E}	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

<Core Design>

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		Title: Swith-1	
Size	Document Number	Rev	
Custom	Vostro Calpella	SA	
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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserve

Size

A3

Document Number

Vostro Calpella

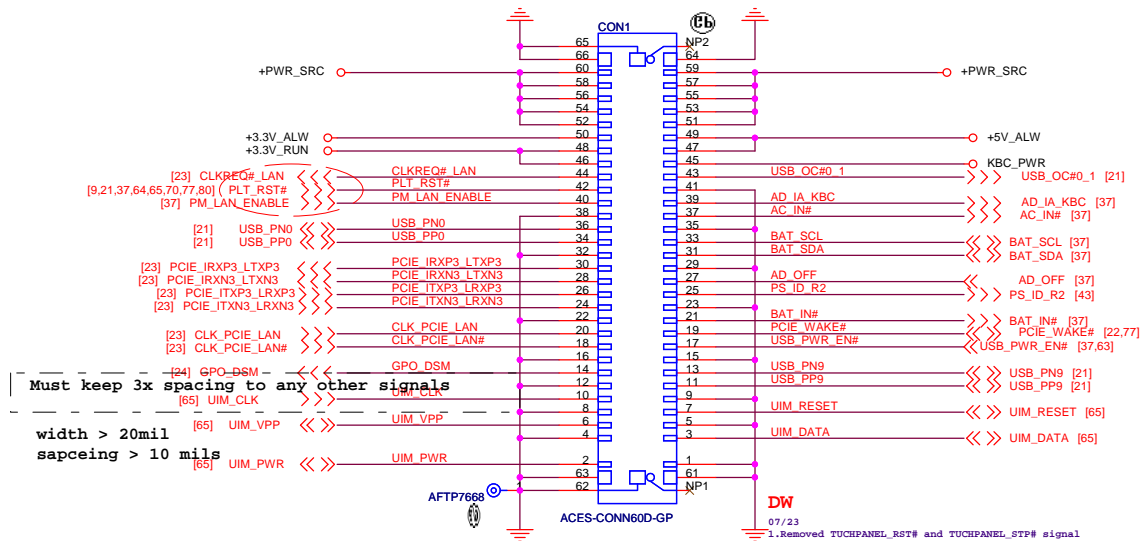
Rev

SA

Date: Wednesday, September 09, 2009

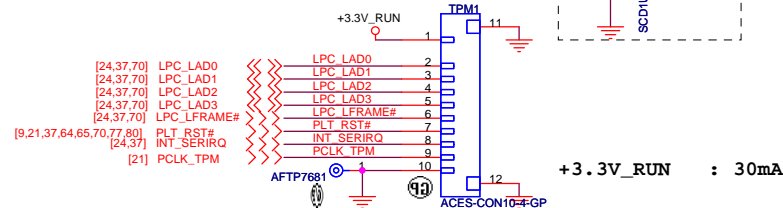
Sheet 75 of 88

DC_IN board CON

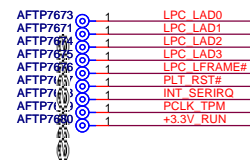


20.F1009.060

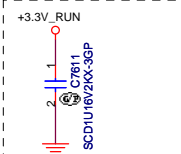
TPM board CON



20.K0238.010

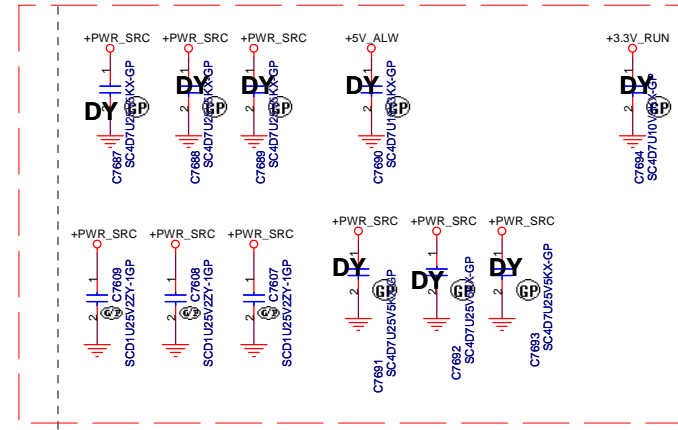
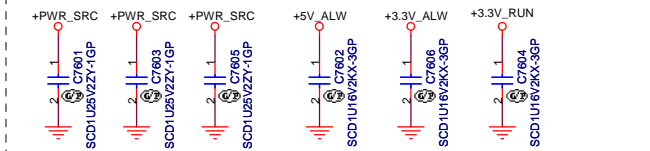


Place near TPM1



+3.3V_RUN : 30mA

Place near CON1



+5V_ALW : 2000mA

+3.3V_ALW : 347mV

+3.3V_RUN : 80mA

+3.3V_RTC_LDO : < 1mA

```
+PWR_SRC    : Estimated by using battery 11.1V,85W
```

DW

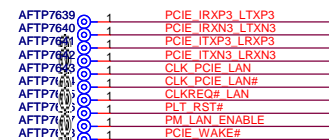
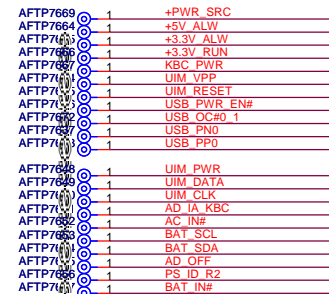
07/2

```
1.Added Power decoupling capacitor pre-0.5A ( 0402*1
0603 *1 )
```

07/2
2. C

07/31
 8 - Change 4 7:14:41M 8.5V 0605 to 0603 for cost

batt



<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DC IN/TPM board CON
-------	----------------------------

Size	Document Number	Rev
Custom	Vostro Calpella	SA

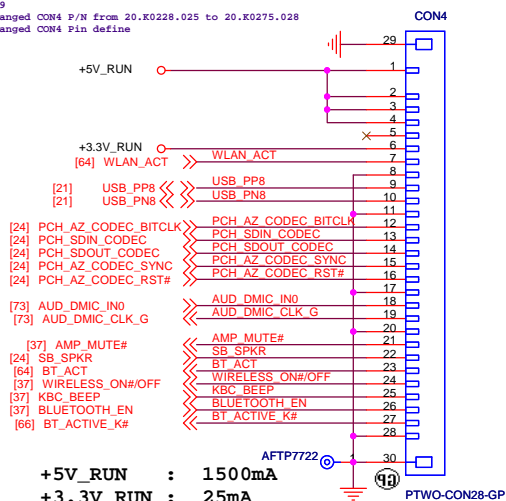
Date: Wednesday, September 09, 2009	Sheet 76 of 88
-------------------------------------	----------------

SSID = User.Interface

DW

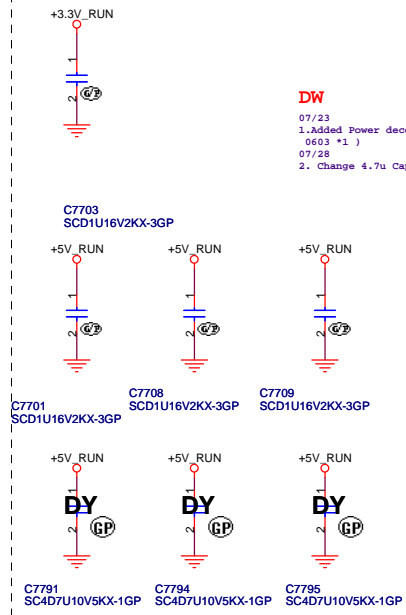
07/08 Not reserve
1. Not reserve BLUETOOTH_DET ??
07/15 Change Power rail
1. Changed CON4.4 per rail from +1.5V_RUN to +15V_ALW
07/23
1. Removed +15V_ALW
07/29
1. Changed CON4 P/N from 20.K0228.025 to 20.K0275.028
1. Changed CON4 Pin define

Audio board CON



20.K0275.028

Place near CON4

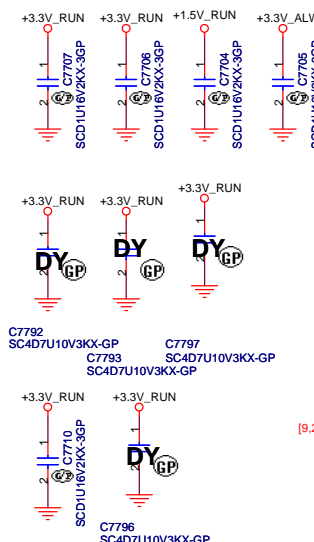


AFTP7710 1 +5V_RUN
AFTP7706 1 +3.3V_RUN
AFTP7708 1 WIRELESS_ON#/OFF
AFTP7702 1 WLAN_ACT
AFTP7703 1 BLUETOOTH_EN
AFTP7704 1 BT_ACTIVE_K#
AFTP7705 1 BT_ACT
AFTP7707 1 USB_PP8
AFTP7708 1 USB_PN8
AFTP7712 1 PCH_AZ_CODEC_BITCLK
AFTP7713 1 PCH_SDIN_CODE
AFTP7714 1 PCH_SDOOUT_CODE
AFTP7715 1 PCH_AZ_CODEC_SYNC
AFTP7716 1 PCH_AZ_CODEC_RST#
AFTP7718 1 SB_SPKR
AFTP7719 1 KBC_BEEP
AFTP7720 1 AUD_DMIC_IN0
AFTP7721 1 AUD_DMIC_CLK_G
AFTP7723 1 AMP_MUTE#

DW

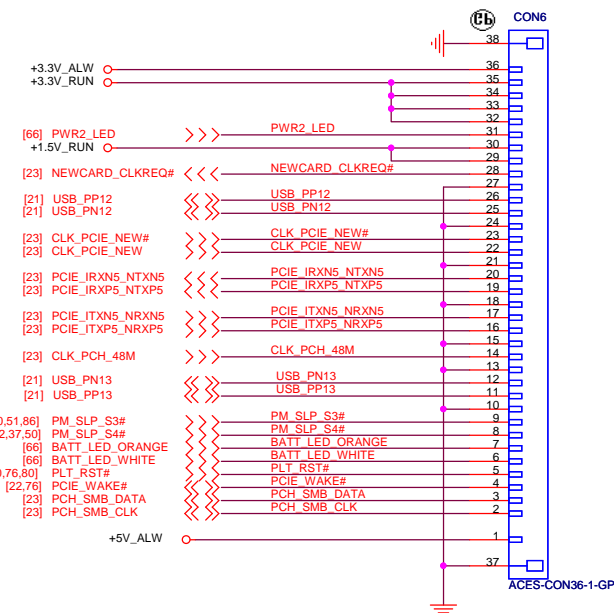
07/23
1. Added Power decoupling capacitor pre-0.5A (0402*1
0603 *1)
07/28
2. Change 4.7u Capacitor from 0603 to 0805, for cost

Place near CON6



AFTP7758 1 +3.3V_ALW
AFTP7757 1 +3.3V_RUN
AFTP7760 1 +1.5V_RUN
AFTP7762 1 USB_PN12
AFTP7759 1 USB_PP12
AFTP7769 1 NEWCARD_CLKREQ#
AFTP7768 1 PCH_SMB_CLK
AFTP7767 1 PCH_SMB_DATA
AFTP7777 1 PM_SLP_S3#
AFTP7776 1 PM_SLP_S4#
AFTP7773 1 BATT_LED_ORANGE
AFTP7772 1 PWR2_LED
AFTP7781 1 PLT_RST#
AFTP7785 1 BATT_LED_WHITE
AFTP7787 1 +5V_ALW
AFTP7771 1 CLK_PCIE_NEW#
AFTP7770 1 CLK_PCIE_NEW
AFTP7761 1 PCIE_IRXN5_NTXN5
AFTP7765 1 PCIE_IRXP5_NTXP5
AFTP7764 1 PCIE_ITXN5_NRXN5
AFTP7763 1 PCIE_ITXP5_NRXP5
AFTP7775 1 USB_PN13
AFTP7766 1 USB_PP13
AFTP7774 1 PCIE_WAKE#
AFTP7778 1 CLK_PCH_48M

IO board CON



20.K0276.036

DW

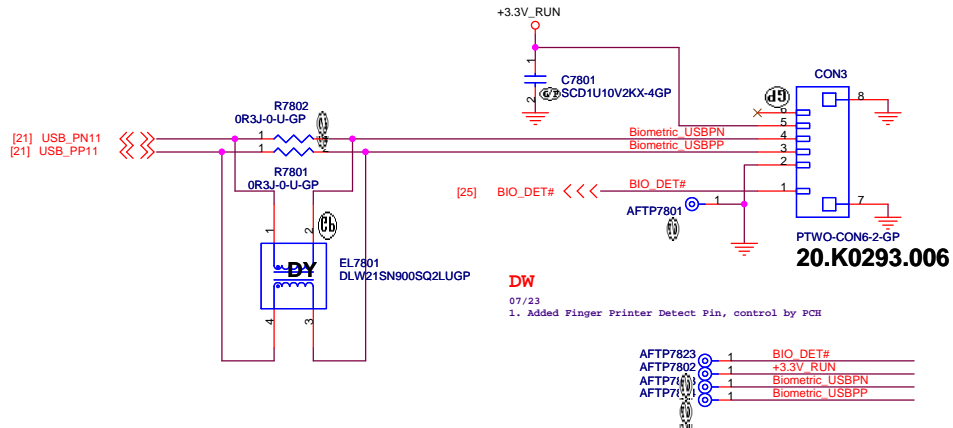
07/10 Change
1. Change CON6 pin define, For Layout
07/14 Updated Spec
2. Deleted USB Port-5
07/23
1. Removed +1.5V_RUN Power rail for JMB380
2. Added CardReader Wake# to send Card detect signal for PCH . (Only For JMB380)
3. Change CON6 pin define
07/28
1. Added +5V_ALW Power rail for Change Power & Battery LED
from common-cathode to common-anode
07/29
1. Remove SATA2_ACT_LED
08/05
1. Changed CON6 Pin define
08/11
1. Changed CON6 Pin define
2. Added +5V_ALW for IO board
08/18
1. Added 48M clock for USB CardReader
2. Added PCIE_WAKE# signals for New Card
3. Changed CON6 Pin define

+1.5V_RUN : 650mA
+3.3V_RUN : 1775mA
+3.3V_ALW : 275mA
+5V_ALW : 60mA

<Core Design>

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Audio BD/IO BD CONN			
Size	Document Number	Rev	SA
Custom	Vostro Montevina Discrete		
Date:	Wednesday, September 09, 2009	Sheet	77 of 88

Finger Printer Connector



Added CON5 pin define	2009/05/26
Change CON5 pin define	2009/06/08
Change CON5 Pin define	2009/06/11
Revised CON5 Pin define	2009/06/17

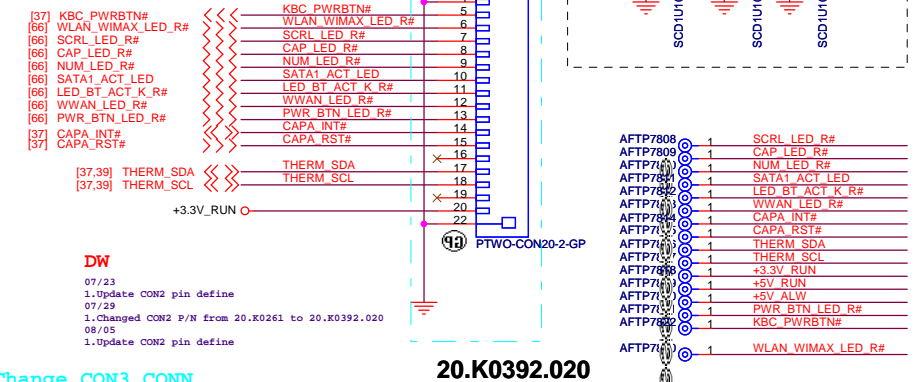
DW

07/10 Added
1.Added Felica Connector

08/11 Removed
1.Remored Felica Connector

LED&Capacity board CONN

Change LED
signal name
2009/06/01



```
Change CON3 CONN
2009/06/01
Update CON pin define
2009/06/04
1. Moved 33ohm resistor, ESD diode to capacity BD
2. NC capacity BD RST pin
2009/06/09
Assign CAPA_RST# GPIO
2009/06/15
```

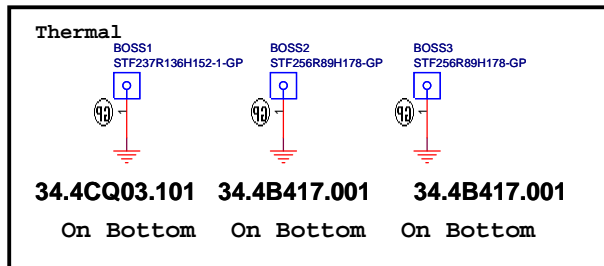
+3.3V_RUN	:	3.5mA
+5V_RUN	:	240mA
+5V_ALW	:	80mA

<Core Design>

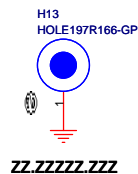


SSID = Mechanical

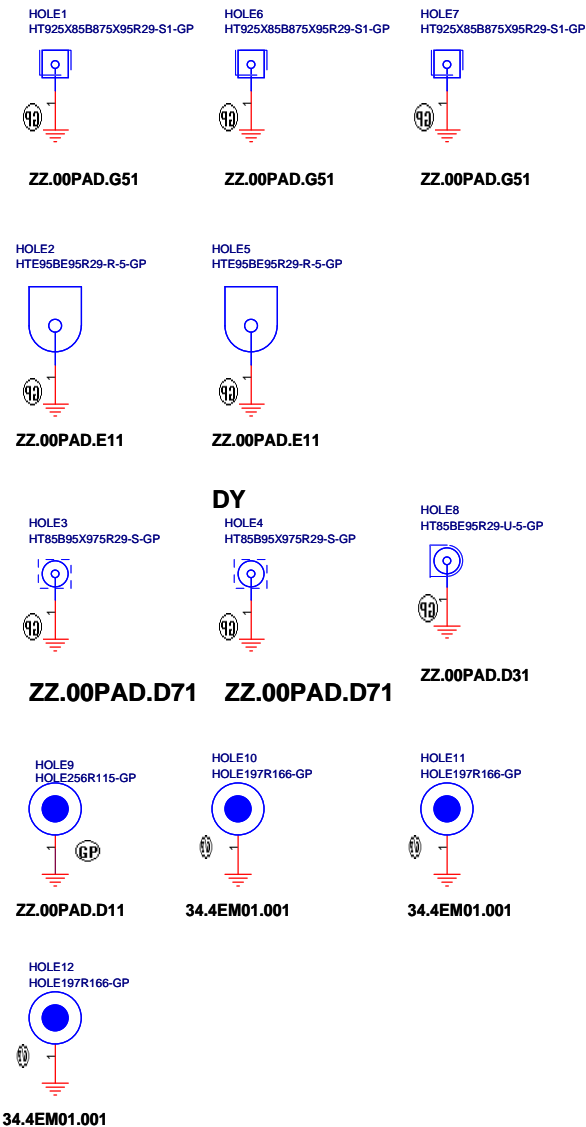
BOSS:



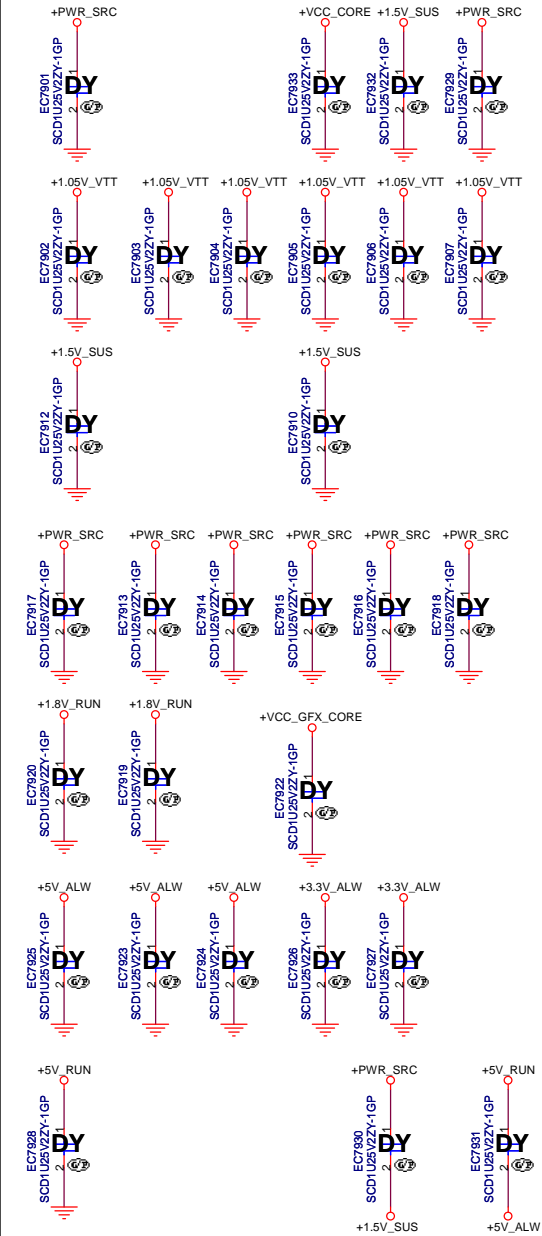
Boss modify 2009/07/23



HOLE:



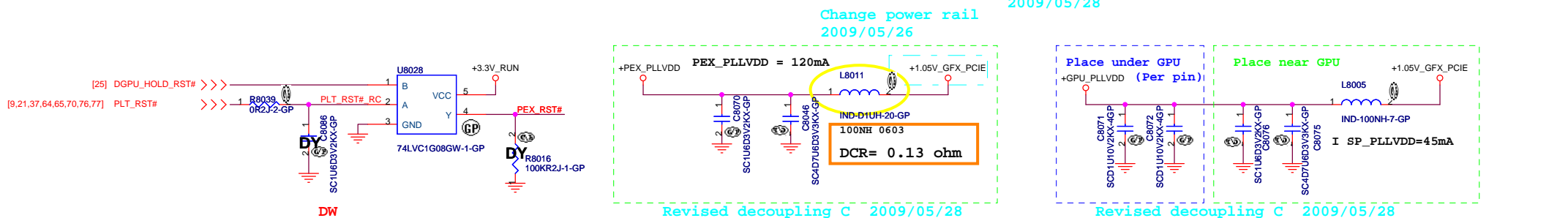
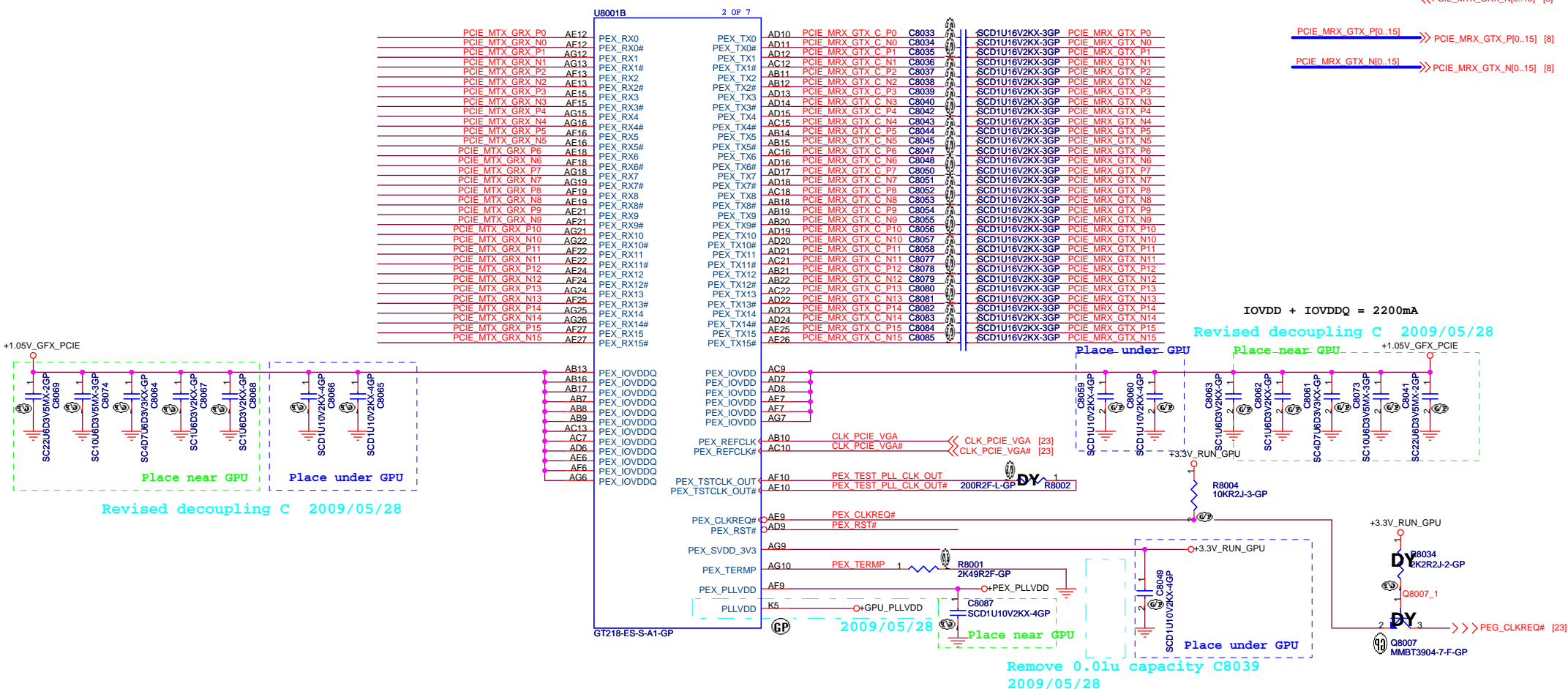
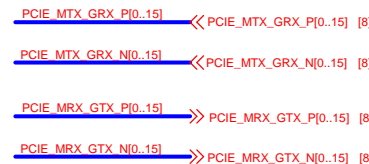
EMI Request



<Core Design>

DELL Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Size Document Number Rev		
Custom Vostro Calpella SA		
Date: Wednesday, September 09, 2009 Sheet 79 of 88		

SSID = VIDEO



<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
VGA-PCIE/LVDS(1/4)			
Size A3	Document Number		Rev S.
Vostro Calpella			
Date:	Wednesday, September 09, 2009	Sheet 80 of 88	

SSID = VIDEO

DW

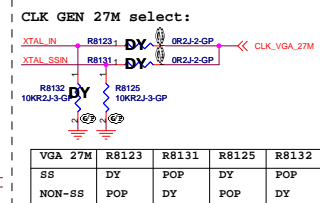
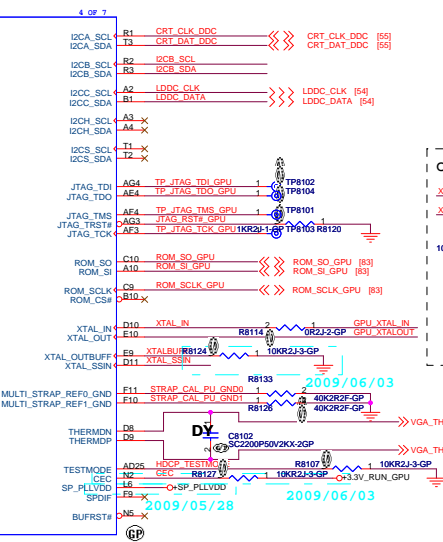
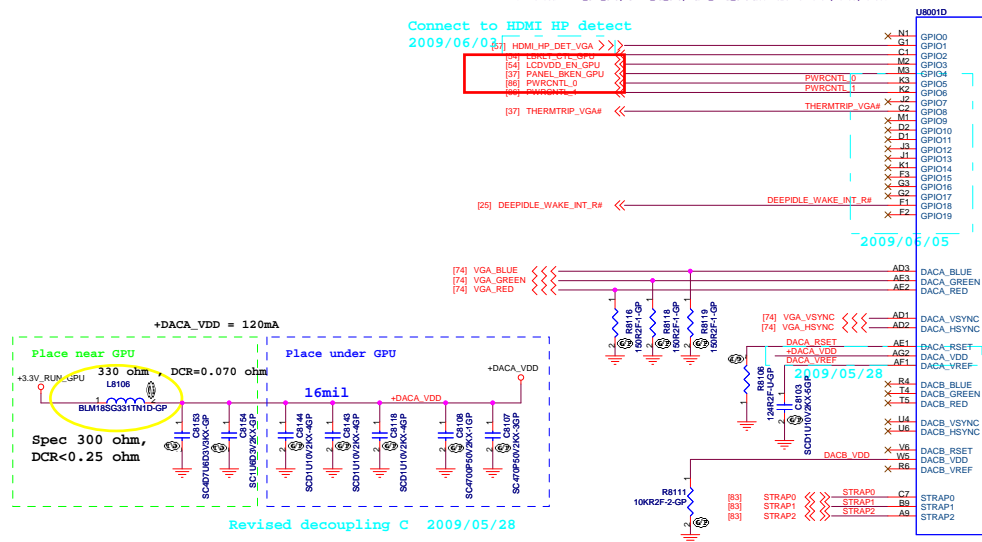
07/05

1. LCD brightness control are separated by GPU,PCH,EC
2. LCD Power Enable control are separated by GPU,PCH,EC
3. LCD Backlight On/Off Status are separated by GPU,PCH,EC

07/10 Not Reserve

1. Shorted LSKLT_CTL1.GPU,LCDVDD_EN.GPU,PANEL_BKRN.GPU Not Reserve R8134,R8135,R8136

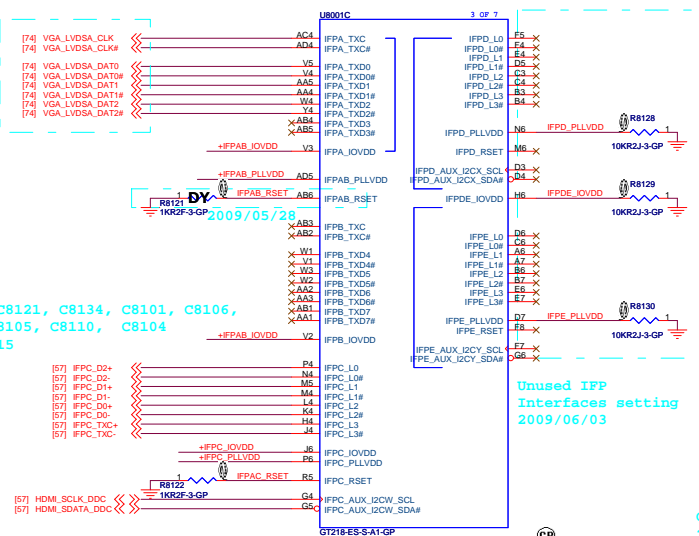
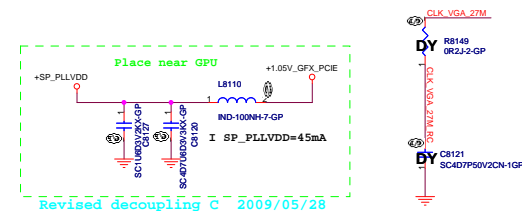
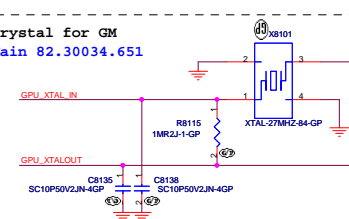
Connect to HDMI HP detect
2009/06/03 [57] HDMI_HP_DET_VGA >>>



```
Added CLK GEN 27M select circuit 2009/06/15
Added R8132 (DY) 2009/06/17
```

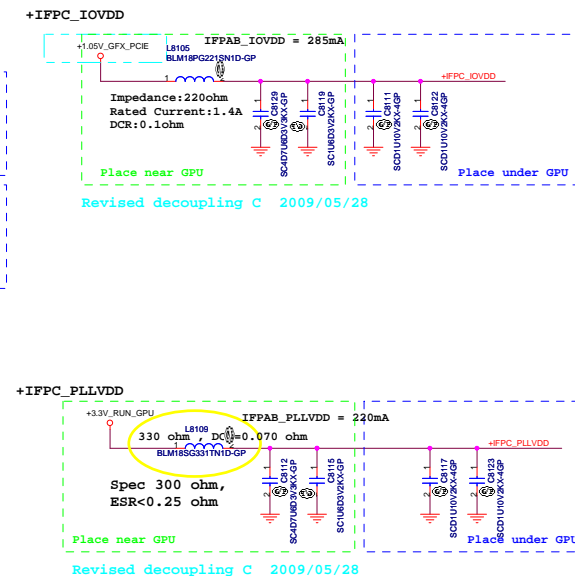
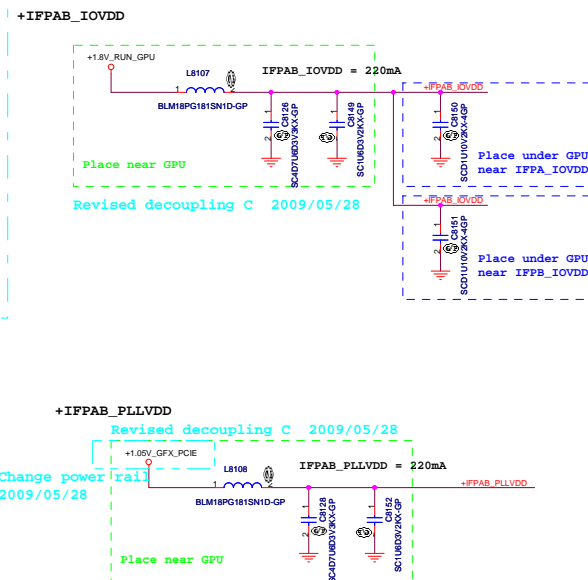
Default X'TAL

```
| Crystal for GM
| Main 82.30034.
```



Removed C8121, C8134, C8101, C8106,
C8114, C8105, C8110, C8104
2009/06/15

Unused IFP
Interfaces setting
2009/06/03



<Core Design:



Title		VGA-LVDS/CRT/DP PORT	
Size A2	Document Number	Vostro Calpella	
Date:	Wednesday, September 09, 2009	Sheet	81 of 88

SSID = VIDEO

[84,85] MDA[0..63]

U8001A

1 OF 7

MDA0 D22 FBA_D0
MDA1 D22 FBA_D1
MDA2 D22 FBA_D2
MDA3 D26 FBA_D3
MDA4 D27 FBA_D4
MDA5 C27 FBA_D5
MDA6 C27 FBA_D6
MDA7 B27 FBA_D7
MDA8 A21 FBA_D8
MDA9 B21 FBA_D9
MDA10 C21 FBA_D10
MDA11 C19 FBA_D11
MDA12 C18 FBA_D12
MDA13 D18 FBA_D13
MDA14 B18 FBA_D14
MDA15 C16 FBA_D15
MDA16 E21 FBA_D16
MDA17 F21 FBA_D17
MDA18 D20 FBA_D18
MDA19 F20 FBA_D19
MDA20 D17 FBA_D20
MDA21 F18 FBA_D21
MDA22 E16 FBA_D22
MDA23 A22 FBA_D23
MDA24 C24 FBA_D24
MDA25 D21 FBA_D25
MDA26 D21 FBA_D26
MDA27 C22 FBA_D27
MDA28 A25 FBA_D28
MDA29 W27 FBA_D29
MDA30 W26 FBA_D30
MDA31 W25 FBA_D31
MDA32 AB25 FBA_D32
MDA33 AB26 FBA_D33
MDA34 AD27 FBA_D34
MDA35 V25 FBA_D35
MDA36 R25 FBA_D36
MDA37 R25 FBA_D37
MDA38 W27 FBA_D38
MDA39 W26 FBA_D39
MDA40 W25 FBA_D40
MDA41 AB25 FBA_D41
MDA42 AB26 FBA_D42
MDA43 AD27 FBA_D43
MDA44 V25 FBA_D44
MDA45 R25 FBA_D45
MDA46 R25 FBA_D46
MDA47 W27 FBA_D47
MDA48 W26 FBA_D48
MDA49 W25 FBA_D49
MDA50 W24 FBA_D50
MDA51 W23 FBA_D51
MDA52 AB25 FBA_D52
MDA53 AB26 FBA_D53
MDA54 AD27 FBA_D54
MDA55 V25 FBA_D55
MDA56 R25 FBA_D56
MDA57 R25 FBA_D57
MDA58 W27 FBA_D58
MDA59 W26 FBA_D59
MDA60 W25 FBA_D60
MDA61 W24 FBA_D61
MDA62 W23 FBA_D62
MDA63 N26 FBA_D63

F26 FBA_CMD_0 <<> FBA_CMD_0 [84]
J24 FBA_CMD_1 <<> FBA_CMD_1 [84,85]
F26 FBA_CMD_2 <<> FBA_CMD_2 [84]
M23 BA1 <<> FBA_CMD_3 [84,85]
N27 FBA_CMD_4 <<> FBA_CMD_4 [85]
M27 FBA_CMD_5 <<> FBA_CMD_5 [85]
K26 FBA_CMD_6 <<> FBA_CMD_6 [85]
J25 FBA_CMD_7 <<> FBA_CMD_7 [85]
J27 FBA_CMD_8 <<> FBA_CMD_8 [85]
Q23 MAA11 <<> MAA11 [84,85]
G26 CAS# <<> CAS# [84,85]
J23 WE# <<> WE# [84,85]
M25 BA0 <<> BA0 [84,85]
K27 FBA_CMD_13 <<> FBA_CMD_13 [85]
G25 MAA12 <<> MAA12 [84,85]
L24 MEM_RST <<> MEM_RST [84,85]
K24 MAA7 <<> MAA7 [84,85]
K24 MAA10 <<> MAA10 [84,85]
G22 FBA_CMD_18 <<> FBA_CMD_18 [84]
K25 MAA0 <<> MAA0 [84,85]
H22 MAA9 <<> MAA9 [84,85]
M26 FBA_CMD_22 <<> FBA_CMD_22 [84]
L24 MAA8 <<> MAA8 [84,85]
F27 FBA_CMD_24 <<> FBA_CMD_24 [84]
G24 MAA1 <<> MAA1 [84,85]
G27 MAA13 <<> MAA13 [84,85]
M24 BA2 <<> BA2 [84,85]
K22 FBA_CMD_28 <<> FBA_CMD_28 [85]
J22 FBA_CMD_29 <<> FBA_CMD_29 [84]
L22 FBA_CMD_30 <<> FBA_CMD_30 [84]

C26 DQMA#0 <<> DQMA#0 [84]
B19 DQMA#1 <<> DQMA#1 [84]
D19 DQMA#2 <<> DQMA#2 [84]
D23 DQMA#3 <<> DQMA#3 [84]
T24 DQMA#4 <<> DQMA#4 [85]
AA23 DQMA#5 <<> DQMA#5 [85]
AB27 DQMA#6 <<> DQMA#6 [85]
T26 DQMA#7 <<> DQMA#7 [85]

D25 QSA#0 <<> QSA#0 [84]
A18 QSA#1 <<> QSA#1 [84]
E18 QSA#2 <<> QSA#2 [84]
B24 QSA#3 <<> QSA#3 [84]
R22 QSA#4 <<> QSA#4 [85]
Y24 QSA#5 <<> QSA#5 [85]
AA27 QSA#6 <<> QSA#6 [85]
R27 QSA#7 <<> QSA#7 [85]

C25 QSA0 <<> QSA0 [84]
A19 QSA1 <<> QSA1 [84]
E19 QSA2 <<> QSA2 [84]
A24 QSA3 <<> QSA3 [84]
T22 QSA4 <<> QSA4 [85]
AA24 QSA5 <<> QSA5 [85]
AA26 QSA6 <<> QSA6 [85]
T27 QSA7 <<> QSA7 [85]

F24 CLKA0 <<> CLKA0 [84]
F23 CLKA0# <<> CLKA0# [84]
N24 CLKA1 <<> CLKA1 [85]
N23 CLKA1# <<> CLKA1# [85]

F24 CLKA0 <<> CLKA0 [84]
F23 CLKA0# <<> CLKA0# [84]
N24 CLKA1 <<> CLKA1 [85]
N23 CLKA1# <<> CLKA1# [85]

F24 CLKA0 <<> CLKA0 [84]
F23 CLKA0# <<> CLKA0# [84]
N24 CLKA1 <<> CLKA1 [85]
N23 CLKA1# <<> CLKA1# [85]

F24 CLKA0 <<> CLKA0 [84]
F23 CLKA0# <<> CLKA0# [84]
N24 CLKA1 <<> CLKA1 [85]
N23 CLKA1# <<> CLKA1# [85]

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F23 CLKA0# <<> CLKA0# [84]
N24 CLKA1 <<> CLKA1 [85]
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F24 CLKA0 <<> CLKA0 [84]
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N24 CLKA1 <<> CLKA1 [85]
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F24 CLKA0 <<> CLKA0 [84]
F23 CLKA0# <<> CLKA0# [84]
N24 CLKA1 <<> CLKA1 [85]
N23 CLKA1# <<> CLKA1# [85]

F24 CLKA0 <<> CLKA0 [84]
F23 CLKA0# <<> CLKA0# [84]
N24 CLKA1 <<> CLKA1 [85]
N23 CLKA1# <<> CLKA1# [85]

Strap pin resistor need use 1% resistor (NV Design Guide)

+3.3V_RUN_GPU

Revised Strap pin setting
2009/06/05
Change R8302 to 34.8K
2009/06/08

Strap pin define

[81] STRAP0 <<> STRAP0
[81] STRAP1 <<> STRAP1
[81] STRAP2 <<> STRAP2
[81] ROM_SCLK_GPU <<> ROM_SCLK_GPU
[81] ROM_SI_GPU <<> ROM_SI_GPU
[81] ROM_SO_GPU <<> ROM_SO_GPU

Logical Strap Bit Mapping
Resistor Pull-Up Pull-Down
5Kohms 1000 0000
10Kohms 1001 0001
15Kohms 1010 0010
20Kohms 1011 0011
25Kohms 1100 0100
30Kohms 1101 0101
35Kohms 1110 0110
45Kohms 1111 0111

Strap0 Strap1 Strap2
USER_BIT0 1 3GIO_PADCFG_LUT_ADR0 0 PCI_DEVID_0 1
USER_BIT1 1 3GIO_PADCFG_LUT_ADR1 1 PCI_DEVID_1 0
USER_BIT2 1 3GIO_PADCFG_LUT_ADR2 1 PCI_DEVID_2 1
USER_BIT3 1 3GIO_PADCFG_LUT_ADR3 1 PCI_DEVID_3 0

EDID is used Reserved N11M-GE1 GPU Device ID=0x0A75

ROM_SI_GPU ROM_SO_GPU ROM_SCLK_GPU
RAM_CFG0 VGA_DEVICE 1 PEX_PLL_EN_TERM 0
RAM_CFG1 SMB_ALT_ADDR 0 SLOT_CLK_CONFIG 1
RAM_CFG2 FB_0_BAR_SIZE 0 SUB_VENDOR 0
RAM_CFG3 XCLK_417 0 PCI_DEVID_4 1

Default setting: SAMSUNG sDDR3 64Mx16BIT-->20K pull down (0x0011)

RAM_CFG[3:0] Config FB_BUS Width Definitions
0000
0001
0010 64MX16 DDR3 64Bit Hynix
0011 64MX16 DDR3 64Bit Samsung Default
0100
0101
0110
0111
0111

If use Hynix sDDR3 64Mx16BIT(0x0010), R8308 change to 15K

SUB_VENDOR XCLK_417 PEX_PLL_EN_TERM
0 No VBIOS ROM 0 277MHz(POR) 0 Disable (POR)
1 BIOS ROM present 1 Reserved 1 Enable
3GIO_PADCFG USER[3:0]
0000 Desktop 1111 Use EDID to detect panel settings
1110 Notebook (POR)

SLOT_CLOCK_CFG
0 GPU and MCH do not share a common reference clock
1 GPU and MCH share a common reference clock (POR)

<Core Design>

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichu, Taipei Hsien 221, Taiwan, R.O.C.

VGA-MEMORY/STRAPS(4/4)
Vostro Calpella
Date: Wednesday, September 09, 2009 Sheet 83 of 88

2009/06/05

Revised decoupling C 2009/05/28

FB_CAL_PU_GND A15
FB_CAL_PD_VDDQ B15
FB_CAL_TERM_GND B16

FB_PLLAVDD R19
FB_DLLAVDD T19

FB_PLLAVDD R19
FB_DLLAVDD T19

FB_PLLAVDD R19
FB_DLLAVDD T19

FB_PLLAVDD R19
FB_DLLAVDD T19

FB_PLLAVDD R19
FB_DLLAVDD T19

FB_PLLAVDD R19
FB_DLLAVDD T19

FB_PLLAVDD R19
FB_DLLAVDD T19

FB_PLLAVDD R19
FB_DLLAVDD T19

FB_PLLAVDD R19
FB_DLLAVDD T19

FB_PLLAVDD R19
FB_DLLAVDD T19

FB_PLLAVDD R19
FB_DLLAVDD T19

FB_PLLAVDD R19
FB_DLLAVDD T19

FB_PLLAVDD R19
FB_DLLAVDD T19

FB_PLLAVDD R19
FB_DLLAVDD T19

FB_PLLAVDD R19
FB_DLLAVDD T19

330 ohm, DCR=0.070 ohm

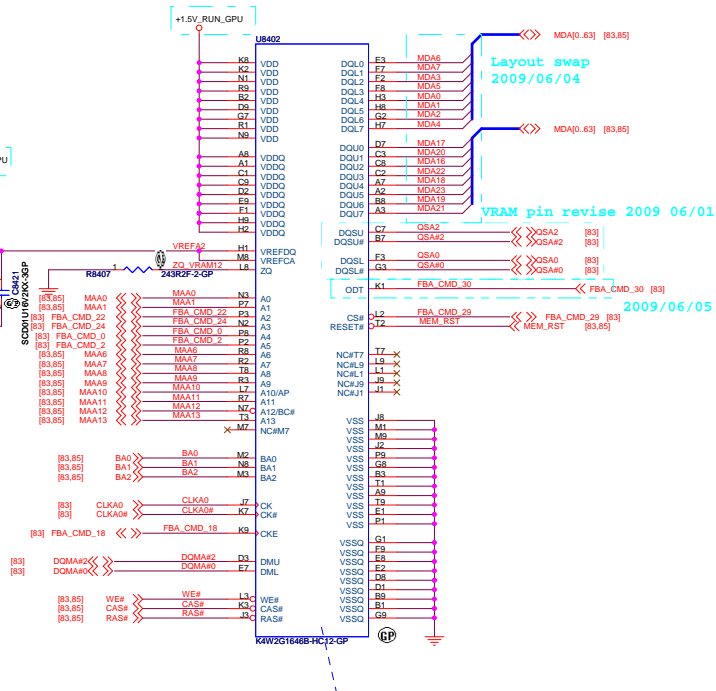
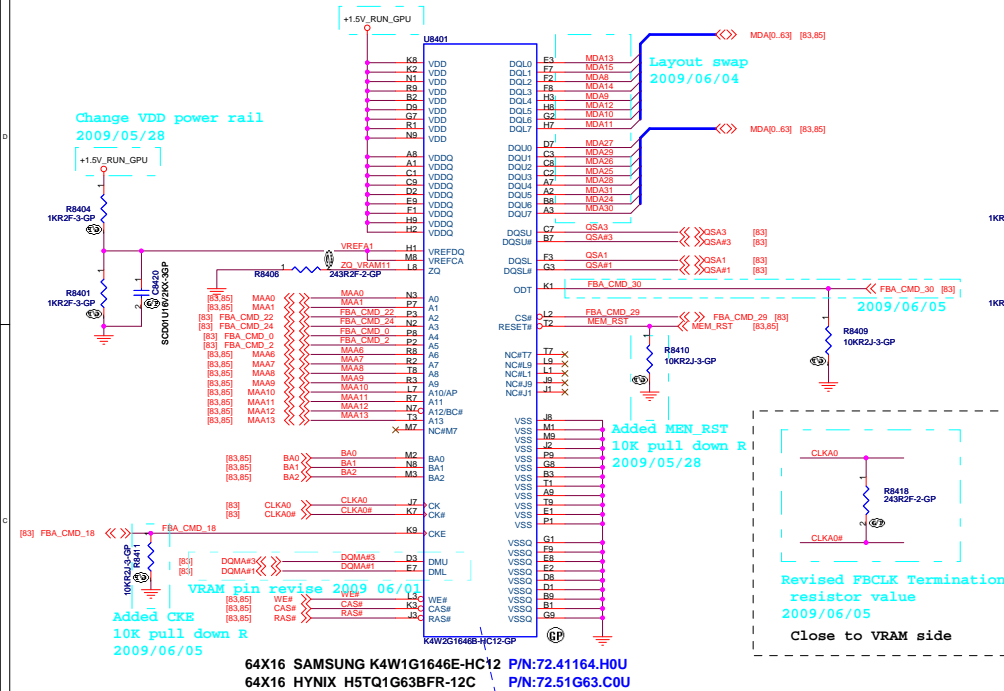
Place near GPU

FB_PLLAVDD+FB_DLLAVDD=100mA

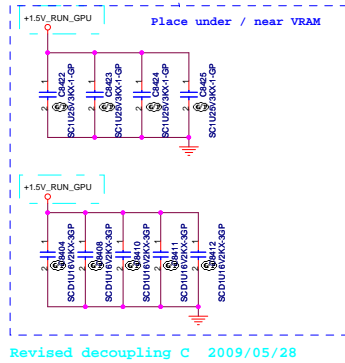
DW

07/10 Updated
1.+FB_PLLVDD power rail corrected to +1.05V_GFX_PCIE

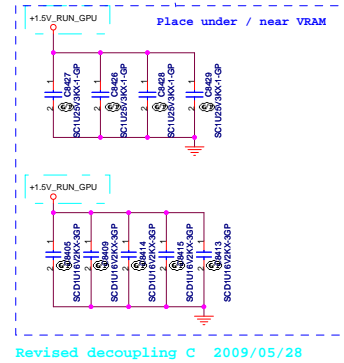
SSID = VIDEO



Change power rail
2009/05/26

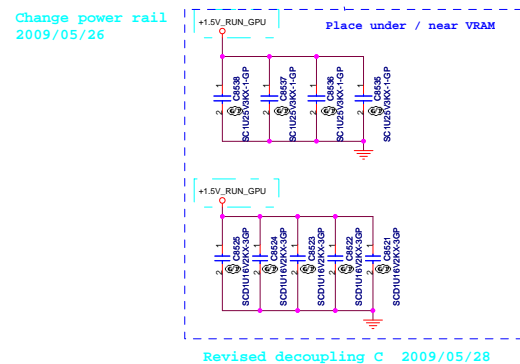
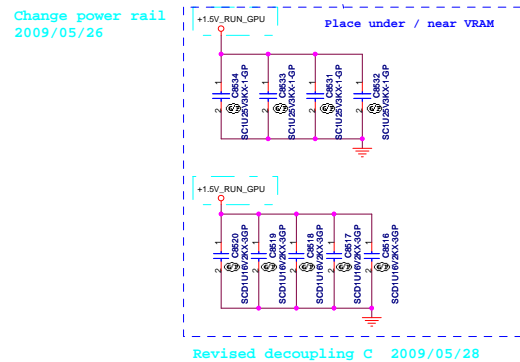
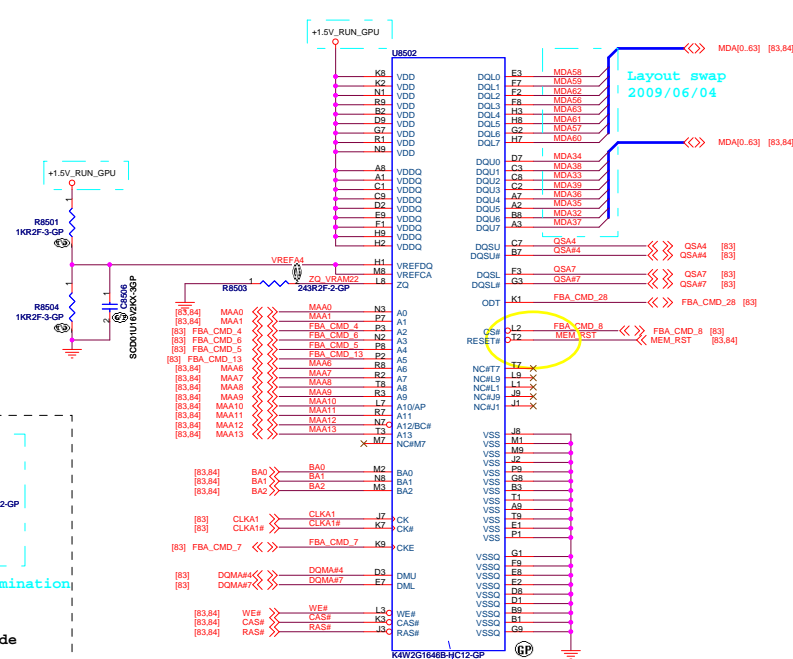
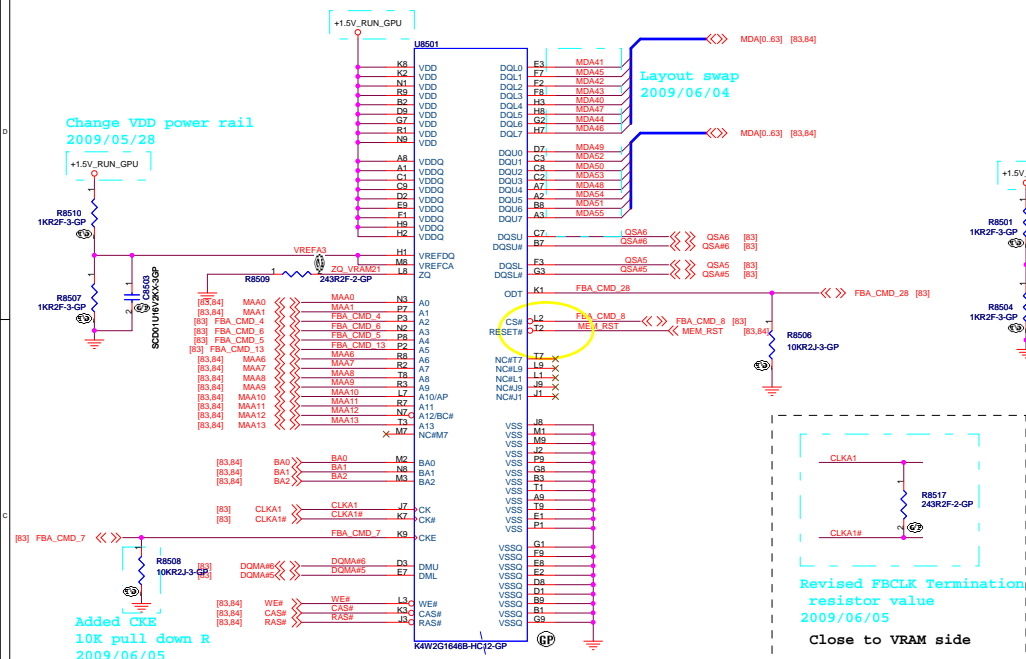


Change power rail
2009/05/26



«Core Design»

SSID = VIDEO



```
SSID = PWR.Plane.Regulator_GFX
```

$$V_{out} = 0.704V * (R1 + R2) / R2$$

DIS
Thermal Design Current = 12.9A
Max Current = 16.77A
18.45A<OCP<21.81A

```

Frequency setting
470K  -->290KHz
200K  -->340KHz
100K  -->380KHz
 39K  -->430KHz

```

470K --> 290KHz

200K --> 340KHz

100K --> 380KHz

39K -->430KHz

PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
H	H	1.03V
H	L	0.85V
L	L	0.8V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCCML04T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/ 11mOhm/14mOhm4.5Vgs/ 84.07686.037
L/S: SIr460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm4.5Vgs/ 84.00460.037
Switching freq-->350KHz

<Core Design>

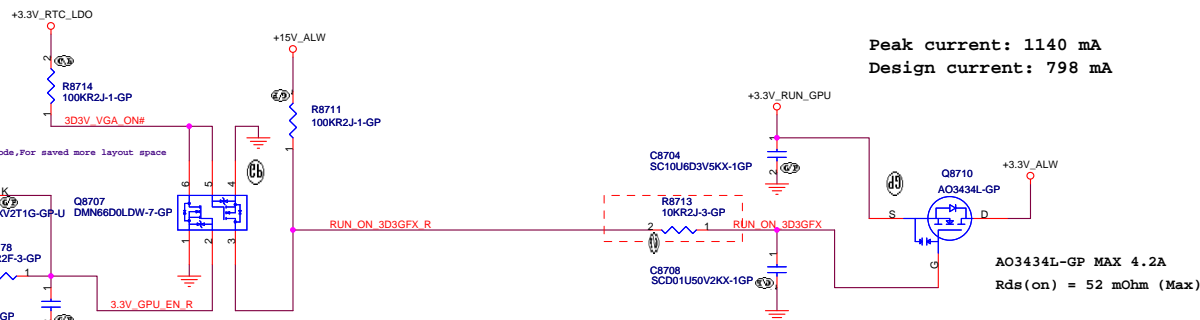


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
TPS51218 +VCC GFX CORE			
Size	Document Number		Rev
Custom	DW Calpella (Discrete)		X0
Date:	Wednesday, September 09, 2009	Sheet 86 of 88	

+3.3V_RUN_GPU

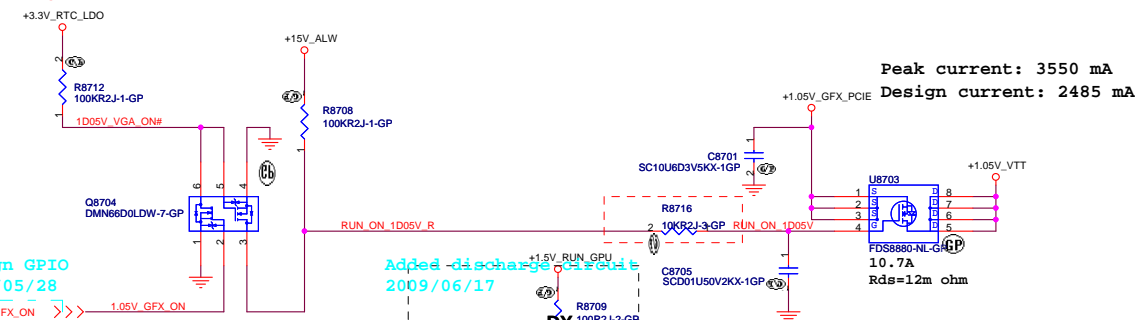
DW
07/30
1. Changed D8706 from 3-Pin to 2-Pin Diode, For saved more layout space



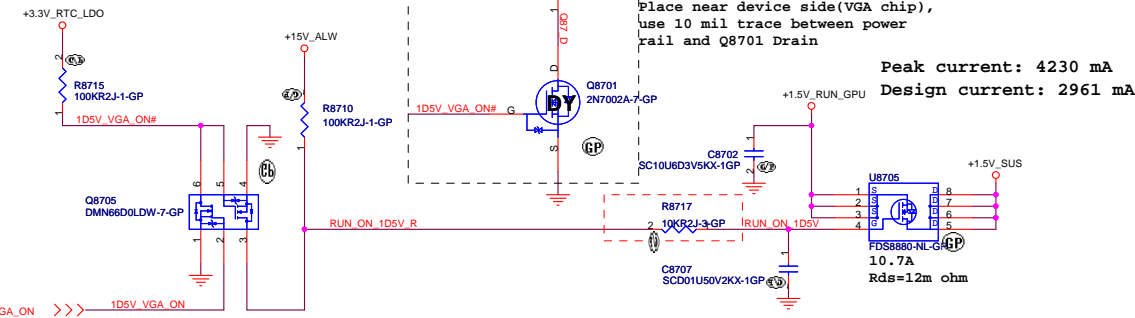
+1.05V_GFX_PCIE:

assign GPIO
2009/05/28

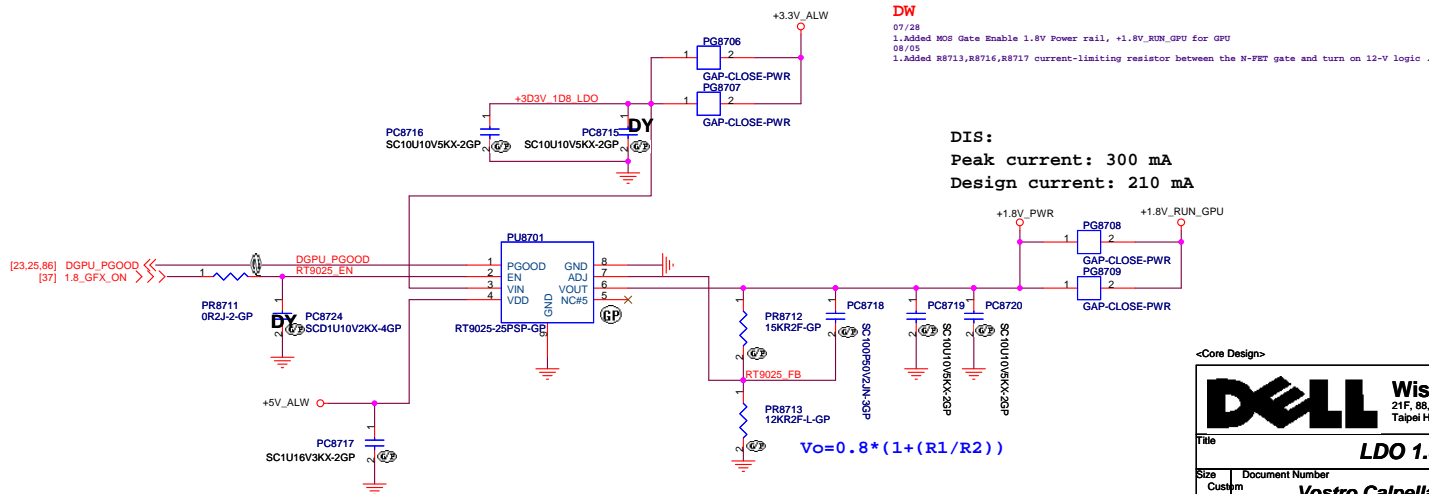
Added discharge circuit
2009/06/17



+1.5V_RUN_GPU:



+1.8V_RUN_GPU



DW
07/28
1. Added MOS Gate Enable 1.8V Power rail, +1.8V_RUN_GPU for GPU
08/05
1. Added R8713, R8716, R8717 current-limiting resistor between the N-FET gate and turn on 12-V logic.

DIS:
Peak current: 300 mA
Design current: 210 mA

$$V_o = 0.8 * (1 + (R1/R2))$$

<Core Design>

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		LDO 1.8V	
Size	Document Number	Rev	
Custom	Vostro Calpella	SA	
Date:	Wednesday, September 09, 2009	Sheet	87 of 88

[illegible]